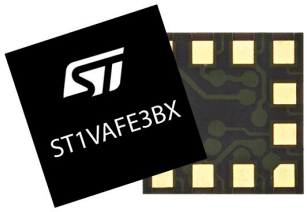
ST1VAFE3BX

Datasheet

Biosensor with vAFE (vertical analog front-end) for biopotential signals and ultralow-power accelerometer with AI and antialiasing



LGA-12L
2.0 x 2.0 x 0.74 (max) mm



Product status link
ST1VAFE3BX

Product summary	
Order code	ST1VAFE3BXTR
Temperature range [°C]	-40 to +85
Package	LGA-12L
Packing	Tape and reel

Product resources
AN6160 (device)
AN6207 (finite state machine)
AN6208 (machine learning core)
AN6173 (ECG monitoring)
TN0018 (handling, mounting, and soldering guidelines)
TN1571 (eSP for cardio monitoring)

Features

- Dual channels for biopotential signal detection and motion tracking
- Supply voltage range from 1.62 V to 3.6 V
  - Independent I/O supply (1.62 V to 3.6 V) for I²C and SPI interfaces
  - Independent I/O supply (extended range: 1.08 V to 3.6 V) for MIPI I3C® interface
- Ultralow supply current at 48.1 µA (typ.) in high-performance mode
  - Power-down: 2.6 µA
- Biopotential signal detection channel with analog hub
  - Single-channel, differential input amplifier (vAFE)
  - Programmable gain and input impedance
  - 12-bit ADC resolution
  - ODR up to 3200 Hz when using analog hub / vAFE channel only
- Accelerometer channel
  - Low noise down to 220 µ*g*/√Hz
  - ±2*g*/±4*g*/±8*g*/±16*g* programmable full-scale
  - ODR from 1.6 Hz to 800 Hz
- Embedded machine learning core
  - For analog hub / vAFE data up to 1.6 kHz
- Programmable finite state machine
  - For analog hub / vAFE data up to 1.6 kHz
- Adaptive self-configuration (ASC) based on the sensor processing output (FSM / MLC)
- Embedded FIFO: up to 128 samples of accelerometer and analog hub / vAFE data or 256 samples of accelerometer data at low resolution
- High-speed I²C/SPI/MIPI I3C® digital output interface
- Advanced pedometer, step detector and step counter
- Self-test
- Small package: 2.0 x 2.0 x 0.74 (max) mm, LGA 12-lead
- 10000 *g* high shock survivability
- ECOPACK and RoHS compliant

Applications

- Biopotential signal detection (ENG, ECG, EEG)
- Wearable and portable devices
- Activity tracking and well-being

Description

The ST1VAFE3BX is a biosensor embedding a vAFE channel to detect biopotential signals and a high-performance 3-axis digital accelerometer for motion tracking.

The device has been designed with a very compact, low-noise, and low-power vAFE with configurable input impedance. The vAFE enables reading analog signals that are complementary to motion signals. The vAFE and motion signals are intrinsically synchronous, so the result is a unique context-aware edge analysis, thus low power and with the minimum possible latency.

Easy integration and actual synchronization of the vAFE with the accelerometer sensor signal allows standalone processing in the MEMS sensor, leveraging its embedded ecosystem, including the FSM and MLC, and offloading the microcontroller.

The device embeds advanced dedicated features and data processing for signal processing like the finite state machine (FSM), adaptive self-configuration (ASC), and machine learning core (MLC) with exportable AI features/filters.

The ST1VAFE3BX MIPI I3C® target interface and embedded 128-level FIFO buffer complete a set of features that make this device a reference in terms of system integration from a standpoint of the bill of materials, processing, or power consumption.

The embedded accelerometer has user-selectable full scales of ±2*g*/±4*g*/±8*g*/±16*g* and is capable of measuring accelerations with output data rates from 1.6 Hz to 800 Hz.

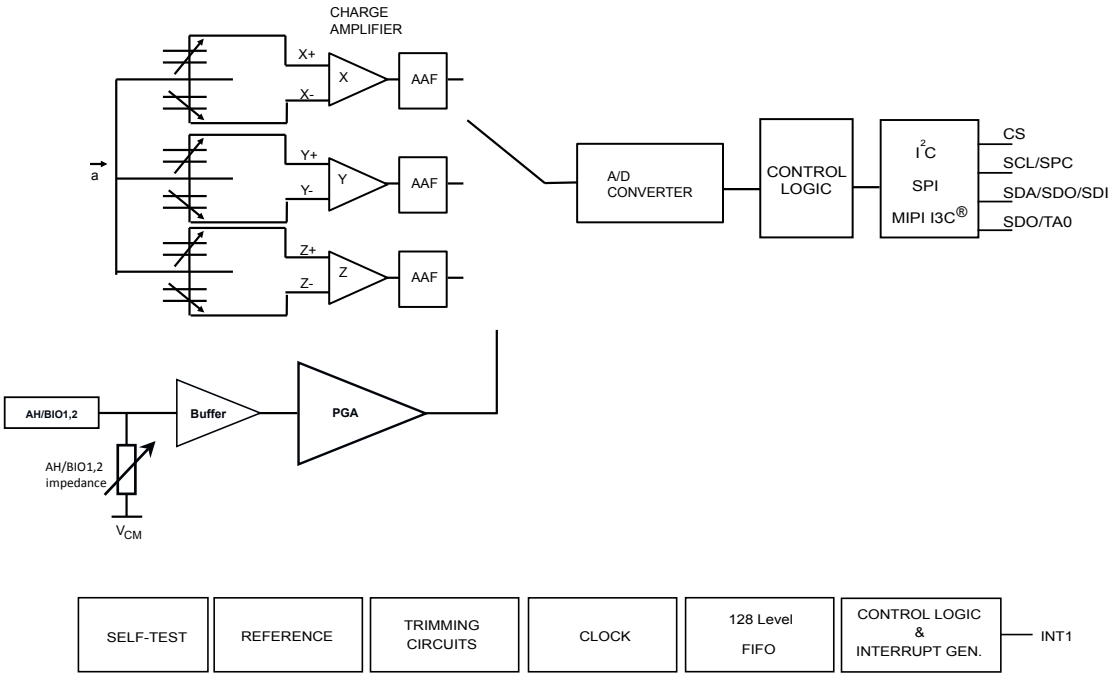
The ST1VAFE3BX has a dedicated internal engine to process motion and acceleration detection including free-fall, wake-up, single/double/triple-tap recognition, activity/inactivity, and 6D/4D orientation.

The ST1VAFE3BX is available in a small thin plastic, land grid array (LGA) package and it is guaranteed to operate over an extended temperature range from -40°C to +85°C.

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

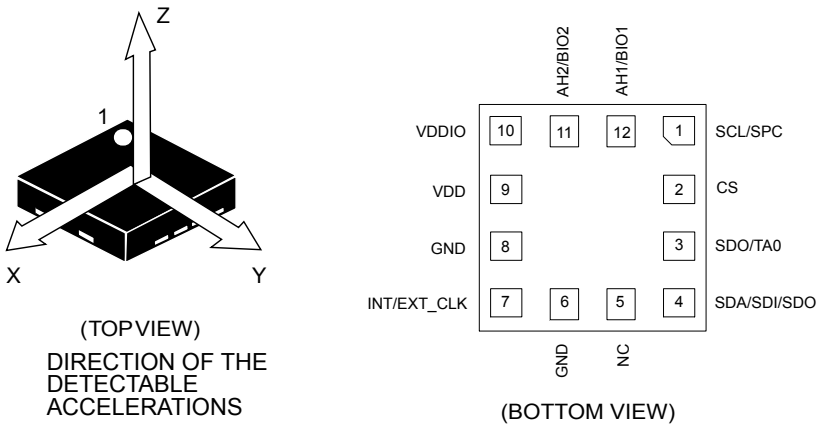


Table 1. Pin description

Pin#	Name	Function
1	SCL SPC	I²C/MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)
2[1]	CS	SPI/I²C/MIPI I3C® mode selection (1: SPI idle mode / I²C/MIPI I3C® enabled; 0: SPI enabled / I²C/MIPI I3C® disabled)
3[2]	SDO TA0	SPI serial data output (SDO) I²C less significant bit of the device address (TA0)
4[2]	SDA SDI SDO	I²C/MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.
6	GND	0 V supply
7	INT/EXT_CLK	Connect to GND if not used as an interrupt pin[3] External clock for synchronization of multiple sensors. This pin has an internal pull-down connected until the INT_PIN_EN bit is set to 1 in register CTRL1 (10h)[4]
8	GND	0 V supply
9	VDD	Power supply
10	VDDIO	Power supply for I/O pins
11[5]	AH2/BIO2	AH input 2 (or BIO electrode 2)
12[5]	AH1/BIO1	AH input 1 (or BIO electrode 1)

1. *The CS pin is internally pulled up by default. The pull-up of the CS pin can be disconnected by setting the bit CS_PU_DIS of register PIN_CTRL (0Ch) to 1.*
2. *The internal pull-up of the SDO/TA0 and SDA/SDI/SDO pins is disconnected by default. The pull-up of the SDO/TA0 pin can be enabled by setting bit SDO_PU_EN of register PIN_CTRL (0Ch) to 1. The pull-up of the SDA/SDI/SDO pin can be enabled by setting bit SDA_PU_EN of register PIN_CTRL (0Ch) to 1.*
3. *When the interrupt flag in the CTRL2 (11h), MD1_CFG (1Fh), EMB_FUNC_INT (0Ah), FSM_INT (0Bh), and MLC_INT (0Dh) registers is set to 1, and the INT_PIN_EN bit of register CTRL1 (10h) is set to 1, the selected interrupt signals are routed to the INT pin.*
4. *When the external clock for the synchronization of multiple sensors is intended to be used, the EXT_CLK_EN bit must be set to 1 in register EXT_CLK_CFG (08h) and the bit INT_PIN_EN set to 0 in register CTRL1 (10h) in order to correctly drive the pin.*
5. *The AH1/BIO1 and AH2/BIO2 pins are internally pulled down by default. The internal pull-down is disconnected when the power-up command is performed, see Section 2.5.1: Power-up command.*

2 Functionality

2.1 Operating modes

When the device is not set in the AH / vAFE only state, the ST1VAFE3BX has four operating modes:

- High-performance mode
- Low-power mode
- Ultralow-power mode
- One-shot mode

In low-power mode, an aggressive antialiasing filter is active, but the overall supply current remains extraordinarily low (refer to Table 4).

When the device is set in the AH / vAFE only state, the ST1VAFE3BX has one operating mode, the active mode (see Section 2.6: Analog hub / vAFE only state).

2.2 Biosensor functionality

The ST1VAFE3BX embeds a vAFE (vertical analog front-end) that is able to detect biopotentials by means of the external electrodes connected to the device. The vAFE can also work as an analog hub, so an analog input can be directly connected to it and converted by the sensing chain of Figure 1. Block diagram to a digital signal for embedded processing, provided that the input source has a common-mode voltage value V_{CM} of 610 mV. Analog hub / vAFE data are available as two's complement data, left-justified in the OUT_AH_BIO_L (2Eh) and OUT_AH_BIO_H (2Fh) registers in 12-bit format at the ODR selected through the ODR[3:0] bits in the CTRL5 (14h) register. The device can be set in a state in which only the AH / vAFE sensor is active by setting the AH_BIO_EN bit of the AH_BIO_CFG2 (31h) register (see Section 2.6: Analog hub / vAFE only state for more information). This condition allows the device to reach a higher ODR (3200 Hz) than what is possible when the accelerometer sensor is enabled as well. In the AH / vAFE only state, if the HP_EN bit in register CTRL3 (12h) is set to 0, the ODR selected is 3200 Hz and the AH / vAFE data is in 12-bit format; otherwise, if the HP_EN bit is set to 1, the ODR selected is 800 Hz and the AH / vAFE data is in 14-bit format. Analog hub / vAFE data can also be processed by MLC/FSM logic.

2.3 vAFE description

The vAFE channel (see Figure 1. Block diagram) consists of an input buffer, having a selectable input impedance, and a programmable gain amplifier (PGA), which also acts as an antialiasing filter for high-gain PGA configuration.

The input buffer, configured through the AH_BIO_MODE[1:0] bits of the AH_BIO_CFG2 (31h) register, is the first stage of the vAFE channel. The fully differential architecture allows rejecting common-mode signals, while having two high-impedance inputs biased at V_{CM}. In single-ended mode, the unused vAFE input is grounded. A forced reset is available, keeping both AH1/BIO1 and AH2/BIO2 pins through low impedance at the reference input voltage V_{CM}.

The input impedance of the vAFE channel ranges from 100 MΩ to 1 GΩ based on the configuration of the AH_BIO_ZIN[1:0] bits of the AH_BIO_CFG2 (31h) register.

The programmable gain amplifier (PGA) is composed of an operational amplifier plus tunable resistors; it amplifies the incoming signal by a selectable factor. Two bits are used to choose from four gain factors: x2, x4, x8, and x16 (bits AH_BIO_GAIN[1:0] of the AH_BIO_CFG2 (31h) register). This stage also acts as an antialiasing filter with a cutoff frequency of 1.6 kHz for the high-gain PGA configuration.

The analog hub / vAFE chain is not compatible with ultralow-power mode.

2.4 One-shot mode

The device features a one-shot mode that can be triggered by the I²C/SPI/I3C digital interface. The sample rate can be customized from "one sample when needed" up to 40 Hz (the antialiasing filter is disabled).

The one-shot mode is not available in the AH / vAFE only state.

2.5 Power-up sequence and active mode configuration

When VDD and VDDIO are set, in order to wake up the device, the first step is to perform a power-up command; the device is now ready to be configured and generate data.

2.5.1 Power-up command

The power-up command, which is different depending on the interface (as described in the following sections), allows the ST1VAFE3BX to enter in power-down and is used to configure the device.

2.5.1.1 I²C/I3C interfaces

If the I²C or I3C interfaces are used, the following sequence should be provided to the device:

- S/Sr+ STATIC ADDRESS+R/W (both R and W sequences are supported).

The device generates a NACK and starts power-up. The operation takes 25 ms (maximum) and once completed, the ST1VAFE3BX is in a power-down state. It is possible to verify the correct transition in the power-down state, providing again the power-up command (S/Sr+ STATIC ADDRESS+R/W) and checking the ACK generation from the device.

To guarantee the current execution of the power-up command, the I²C/I3C controller should operate at open-drain speed using I²C fast mode plus reference timing.

In the ST1VAFE3BX if the bus is at 1.2 V (supported only for I3C) and the device is in power-down, the power-up sequence must be performed in I²C fast mode plus.

If the I3C interface is used, a dynamic address should be assigned before starting device configuration.

2.5.1.2 SPI interface

If the SPI interface is used, set the EN_DEVICE_CONFIG bit to 1 in the EN_DEVICE_CONFIG (3Eh) register in order to use the power-up command. The device starts the power-up and this operation takes 25 ms (maximum). In order to verify that the device has correctly completed the transition to power-down, the who_am_I value (expected to be equal to 48h) can be checked by reading the WHO_AM_I (0Fh) register.

Note: When the power-up command is performed using the SPI interface, the I²C and the I3C interfaces are automatically disabled as soon as the device exits the power-down condition.

2.6 Analog hub / vAFE only state

After executing the power-up command, the device is automatically configured in power-down mode.

When the device is in power-down mode, it can be set in the AH / vAFE only state by setting the AH_BIO_EN bit of the AH_BIO_CFG2 (31h) register.

After the device has been set in the AH / vAFE only state, follow this procedure to set it in active mode:

1. Write 01h in register AH_BIO_CFG3 (32h).
2. Wait 10 ms.
3. Change the HP_EN bit value in register CTRL3 (12h), if necessary.
4. Write 00h in register AH_BIO_CFG3 (32h).
5. Wait 10 ms.
6. Write the desired value in register CTRL5 (14h) to start generating AH / vAFE data at the selected ODR.

When the device is in active mode, it can be set in power-down mode by writing 0000 in the ODR[3:0] bits of the CTRL5 (14h) register.

When the device is in the AH / vAFE only state, the features related to event-detection interrupts, pedometer functions, tilt, and significant motion detection (see Section 6: Digital main blocks and embedded low-power features) are not available.

2.7 Activity/inactivity, Android stationary/motion detection functions

The activity/inactivity function recognizes the device's sleep state and allows reducing system power consumption.

When the activity/inactivity function is activated by setting the SLEEP_ON bit in WAKE_UP_THS (1Ch), the device automatically goes to the inactivity output data rate selected by the INACT_ODR[1:0] bits in register CTRL4 (13h).

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Android stationary/motion detection function only recognizes the device's sleep state.

When the Android stationary/motion detection function is activated by setting to a stationary condition the INACT_ODR[1:0] bits in register CTRL4 (13h), the device detects acceleration below a fixed threshold but does not change the ODR after sleep state detection.

The activity/inactivity recognition and Android stationary/motion detection functions are activated by writing the desired threshold in the WAKE_UP_THS (1Ch) register. The high-pass filter is automatically enabled.

If the device is in sleep (inactivity/stationary) mode, when at least one of the axes exceeds the threshold in WAKE_UP_THS (1Ch), the device goes into a sleep-to-wake state (as wake-up).

For the activity/inactivity function, the device, in a wake-up state, returns to the ODR before sleep state detection.

Activity/inactivity, Android stationary/motion detection threshold and duration can be configured in the following control registers:

WAKE_UP_THS (1Ch)

WAKE_UP_DUR (1Dh)

2.8 Interrupt event recognition

The device may be configured to generate interrupt signals coming from an independent inertial wake-up/free-fall event or from the position of the device itself. The thresholds and timing of this interrupt generator are programmable by the end user in runtime.

Automatic programmable sleep-to-wake-up and return-to-sleep functions are also available for enhanced power saving.

The device interrupts signal can behave as:

- Free-fall: 3-axis underthreshold recognition
- Wake-up: axis recognition
- Wake-to-sleep: change of state recognition active-sleep (also known as activity-inactivity)
- 6D and 4D orientation detection: change of position recognition
- Tap-tap: single/double/triple-tap detection

All these functions are parallel, but during sleep, it is not possible to recognize a tap-tap event. All these signals can be driven to the INT pin through register MD1_CFG (1Fh).

All these functions are enabled by setting the INTERRUPTS_ENABLE bit in register INTERRUPT_CFG (17h) to 1.

It is possible to configure the duration of the interrupt using the LIR bit in INTERRUPT_CFG (17h) as shown in the following table.

Table 2. Configuration of duration of interrupt

LIR	Interrupt type
0	Level mode
1	Latched mode

- Interrupt level mode: the interrupt signal goes high when an interrupt event occurs and is reset when the acceleration data fall below the threshold.
- Interrupt latched mode: the interrupt signal on the INT pin is the OR of the interrupt flags enabled through the MD1_CFG (1Fh) register. Each interrupt flag goes to 1 when an interrupt event occurs and is reset when the dedicated source register is read. The interrupt generator block is inhibited 1 ODR after the reset event. It is possible to reset all the interrupt flags simultaneously by reading the ALL_INT_SRC (24h) register.

3 Electrical and mechanical specifications

3.1 Electrical characteristics

@VDD = 1.8 V, T = 25°C unless otherwise noted.

The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.

Table 3. Electrical parameters of analog hub / vAFE (@VDD = 1.8 V, T = 25°C)

Parameter	Test conditions		Min.	Typ.(1)	Max.	Unit
ODR in AH / vAFE only state(2)	Configurable		800		3200	Hz
Input range	DC coupled	PGA gain = 2		±200		mV
		PGA gain = 16		±25		
Offset	Input referred			±1		mV
Noise	Shorted input, gain = 16, BW = [20 ÷ 400 Hz], input referred			10		μV_{RMS}
AH / vAFE channel gain	PGA gain = 16, 16 bits, input referred			1311		LSB/mV
Channel gain	AH_BIO_GAIN_[1:0] = 00			2		V/V
	AH_BIO_GAIN_[1:0] = 01			4		
	AH_BIO_GAIN_[1:0] = 10			8		
	AH_BIO_GAIN_[1:0] = 11			16		
Input common mode				0.61		V
CMRR	50 Ω source impedance, sinusoidal input (freq. 50/60 Hz, amp. 100 mV peak to peak), PGA gain = 2			80		dB
Input impedance	AH_BIO_C_ZIN_[1:0] = 00			100		MΩ
	AH_BIO_C_ZIN_[1:0] = 01			200		
	AH_BIO_C_ZIN_[1:0] = 10			500		
	AH_BIO_C_ZIN_[1:0] = 11			1000		
Selectable bandwidth in AH / vAFE only state(2)				45 90 180 360 700 1600		Hz
ADC resolution				12		Bit

1. *VDDIO = 1.8 V. Typical values are based on characterization and are not guaranteed.*
2. *See Table 39 for setting the configuration.*

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ(1)	Max.	Unit
VDD	Supply voltage		1.62	1.8	3.6	V
VDDIO	I/O pins supply voltage	I²C and SPI interfaces	1.62		3.6	V
		MIPI I3C® interface	1.08		3.6	
Idd	Supply current in high-performance mode(2)	FS = ±8 *g* ODR = all ODRs BW = ODR/2 with antialiasing filter		48.1		µA
IddULP	Supply current in ultralow-power mode	FS = ±8 *g* ODR = 1.6 Hz, BW = ODR/2		3.6		µA
IddPD	Supply current in power-down			2.6		µA
V_{IH}	Digital high-level input voltage		0.7*VDDIO			V
V_{IL}	Digital low-level input voltage				0.3*VDDIO	V
V_{OH}	Digital high-level output voltage	I_{OH} = 4 mA(3)	VDDIO - 0.2			V
V_{OL}	Digital low-level output voltage	I_{OL} = 4 mA(3)			0.2	V

1. *Typical specifications are not guaranteed.*
2. *The supply current value is the same for vAFE only or vAFE + accelerometer.*
3. *4 mA is the maximum driving capability, that is, the maximum DC current that can be sourced/sunk by the digital pin in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.*

3.2 Mechanical characteristics

@VDD = 1.8 V, T = 25°C unless otherwise noted.

The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.

Table 5. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
FS	Measurement range			±2		*g*
				±4		
				±8		
				±16		
So	Sensitivity(2)	FS = ±2 *g*		0.061		mg/digit
		FS = ±4 *g*		0.122		
		FS = ±8 *g*		0.244		
		FS = ±16 *g*		0.488		
An	Noise density - high-performance mode	FS = ±8 *g* ODR = 800 Hz, BW = ODR/2		220		µg/√Hz
TyOff	Zero-*g* level offset accuracy(3)			±30		mg
TCO	Zero-*g* offset change vs. temperature			±1		mg/°C
TCS	Sensitivity change vs. temperature			±0.035		%/°C
ST	Self-test positive difference	X-axis	50	-	700	mg
		Y-axis	50	-	700	
		Z-axis	200	-	1200	

1. *Typical specifications are not guaranteed.*
2. *16-bit format*
3. *Values after factory calibration test and trimming*

3.3 Communication interface characteristics

3.3.1 SPI - serial peripheral interface

Subject to general operating conditions for VDD and Top.

Table 6. SPI target timing values

Symbol	Parameter	Value(1)			Unit
		Min	Typ	Max	
$f_{c(SPC)}$	SPI clock frequency			10	MHz
$t_{c(SPC)}$	SPI clock period	100			ns
$t_{high(SPC)}$	SPI clock high	45			
$t_{low(SPC)}$	SPI clock low	45			
$t_{su(CS)}$	CS setup time (mode 3)	5			
	CS setup time (mode 0)	20			
$t_{h(CS)}$	CS hold time (mode 3)	20			
	CS hold time (mode 0)	20			
$t_{su(SI)}$	SDI input setup time	7			
$t_{h(SI)}$	SDI input hold time	15			
$t_{v(SO)}$	SDO valid output time			25	
$t_{dis(SO)}$	SDO output disable time			50	
C_{load}	Bus capacitance			100	pF

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production*

Figure 3. SPI target timing in mode 0

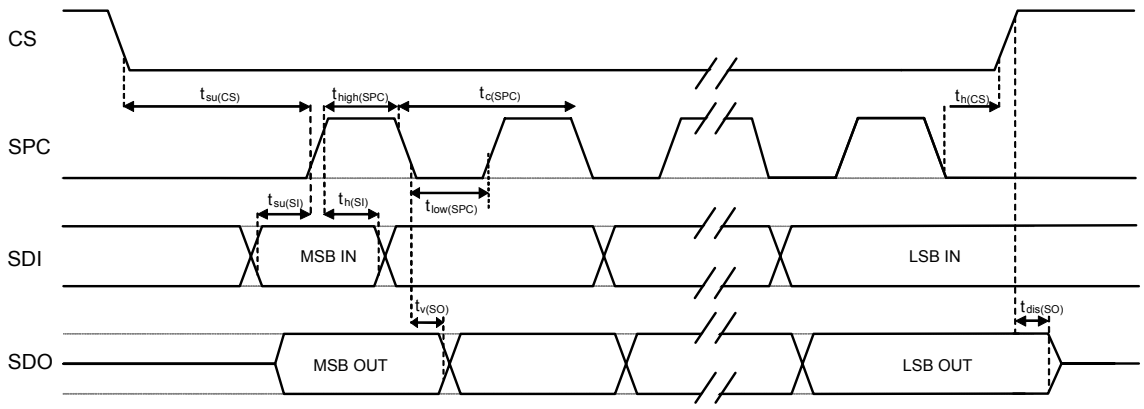
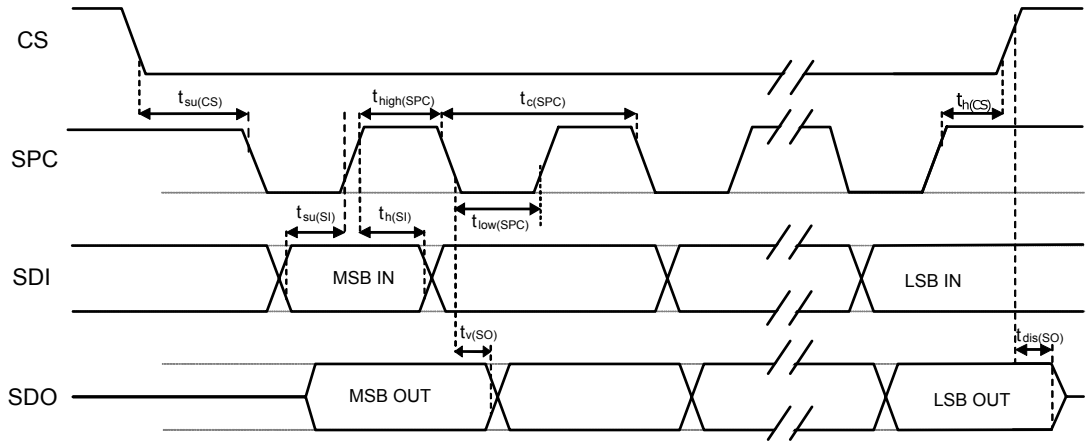


Figure 4. SPI target timing in mode 3



Note: Measurement points are done at 0.3·VDDIO and 0.7·VDDIO for both input and output ports.

3.3.2 I²C - inter-IC control interface

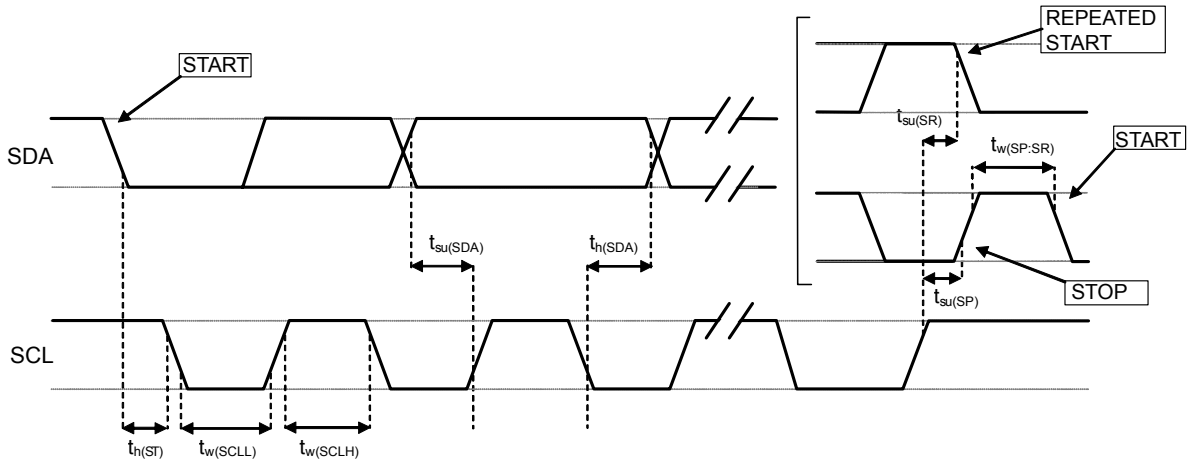
Subject to general operating conditions for VDD and Top.

Table 7. I²C target timing values

Symbol	Parameter	I²C fast mode(1)(2)		I²C fast mode plus(1)(2)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	400	0	1000	kHz
$t_{w(SCLL)}$	SCL clock low time	1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	0.6		0.285		
$t_{su(SDA)}$	SDA setup time	100		50		ns
$t_{h(SDA)}$	SDA data hold time	0	0.9	0		µs
$t_{h(ST)}$	START/REPEATED START condition hold time	0.6		0.26		
$t_{su(SR)}$	REPEATED START condition setup time	0.6		0.26		
$t_{su(SP)}$	STOP condition setup time	0.6		0.26		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	1.3		0.5		
	Data valid time		0.9		0.45	
	Data valid acknowledge time		0.9		0.45	
C_B	Capacitive load for each bus line		400		550	pF

1. *Data based on standard I²C protocol requirement, not tested in production.*
2. *Data for I²C fast mode and I²C fast mode plus have been validated by characterization, not tested in production.*

Figure 5. I²C target timing diagram



Note: Measurement points are done at 0.3·VDDIO and 0.7·VDDIO for both ports.

3.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings		Maximum value	Unit
VDD	Supply voltage		-0.3 to +4.3	V
VDDIO	I/O pins supply voltage		-0.3 to +4.3	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/TA0)		-0.3 to VDDIO +0.3	V
A_{UNP}	Acceleration (any axis, unpowered)		3000 *g* for 0.5 ms	*g*
			10000 *g* for 0.2 ms	*g*
T_{OP}	Operating temperature range		-40 to +85	°C
T_{STG}	Storage temperature range		-40 to +125	°C
ESD	Electrostatic discharge protection	HBM	2	kV
		IEC61000-4-2 contact discharge	8(1)	
		IEC61000-4-2 air-gap discharge	8(1)	

1. *ESD test performed with 5 kΩ series resistor + diode*

Note: Supply voltage on any pin should never exceed 4.3 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3.5 Terminology

3.5.1 Accelerometer sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.5.2 Accelerometer zero-*g* level offset

Zero-*g* level offset describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two’s complement number). A deviation from ideal value in this case is called zero-*g* level offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Zero-*g* level offset change vs. temperature”.

4 Digital interfaces

The registers embedded inside the ST1VAFE3BX may be accessed through both the I²C, MIPI I3C® and SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I²C/MIPI I3C® interface, the CS line must be tied high (that is, connected to VDDIO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	SPI/I²C/MIPI I3C® mode selection 1: SPI idle mode / I²C/MIPI I3C® enabled 0: SPI enabled / I²C/MIPI I3C® disabled
SCL SPC	I²C/MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I²C/MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
TA0 SDO	I²C address selection (TA0) SPI serial data output (SDO)

4.1 I²C serial interface

The ST1VAFE3BX I²C is a bus target. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in the table below.

Table 10. I²C terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Controller	The device that initiates a transfer, generates clock signals, and terminates a transfer
Target	The device addressed by the controller

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to VDDIO through an external pull-up resistor. When the bus is free, both the lines are high.

The I²C interface supports fast mode (400 kHz) and fast mode plus (1000 kHz) I²C standards as well as normal mode.

4.1.1 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the controller, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the target in the first 7 bits and the eighth bit tells whether the controller is receiving data from the target or transmitting data to the target. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the controller.

The target address (TAD) associated to the ST1VAFE3BX is 001100xb where the x bit is modified by the TA0/SDO pin in order to modify the device address. If the TA0/SDO pin is connected to the supply voltage, the address is 0011001b, otherwise if the TA0/SDO pin is connected to ground, the address is 0011000b. This solution permits to connect and address two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver that has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the ST1VAFE3BX behaves like a target device and the following protocol must be adhered to. After the start condition (ST) a target address is sent. Once a target acknowledge (TAK) has been returned, an 8-bit subaddress (SUB) is transmitted: the 7 LSb represents the actual register address while the CTRL1 (10h) (IF_ADD_INC) bit defines the address increment.

The target address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes. If the bit is 0 (write) the controller transmits to the target with direction unchanged. Table 11 explains how the TAD+read/write bit pattern is composed, listing all the possible configurations.

Table 11. TAD+read/write patterns

Command	TAD[6:1]	TAD[0] = TA0	R/W	TAD+R/W
Read	010000	0	1	01000001 (41h)
Write	010000	0	0	01000000 (40h)
Read	010000	1	1	01000011 (43h)
Write	010000	1	0	01000010 (42h)

Table 12. Transfer when controller is writing one byte to target

Controller	ST	TAD + W		SUB		DATA		SP
Target			TAK		TAK		TAK	

Table 13. Transfer when controller is writing multiple bytes to target

Controller	ST	TAD + W		SUB		DATA		DATA		SP
Target			TAK		TAK		TAK		TAK	

Table 14. Transfer when controller is receiving (reading) one byte of data from target

Controller	ST	TAD + W		SUB		SR	TAD + R			NCAK	SP
Target			TAK		TAK			TAK	DATA		

Table 15. Transfer when controller is receiving (reading) multiple bytes of data from target

Controller	ST	TAD+W		SUB		SR	TAD+R			CAK		CAK		NCAK	SP
Target			TAK		TAK			TAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a target receiver does not acknowledge the target address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the target. The controller can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

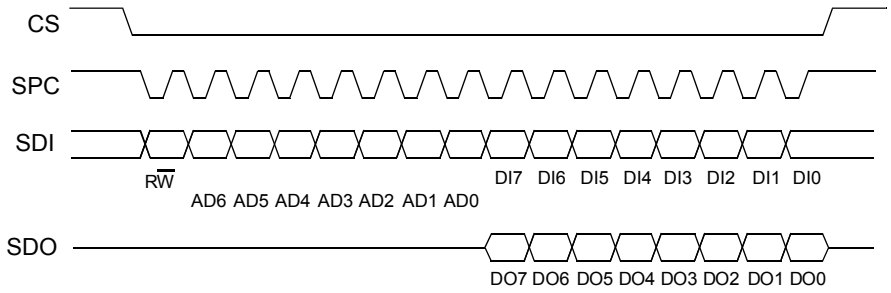
In the presented communication format CAK is controller acknowledge and NCAK is no controller acknowledge.

4.2 SPI bus interface

The ST1VAFE3BX SPI is a bus target. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using 4 wires: **CS**, **SPC**, **SDI**, and **SDO**.

Figure 6. Read and write protocol



CS enables the serial port and it is controlled by the SPI controller. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI controller. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip drives SDO at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

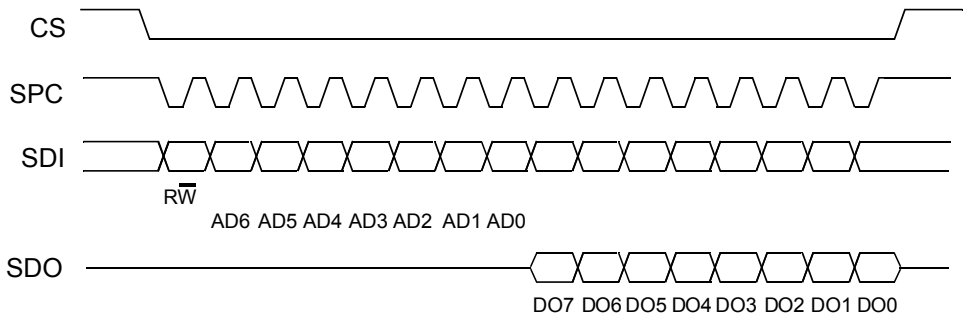
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands additional blocks of 8 clock periods are added. When the CTRL1 (10h) (IF_ADD_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL1 (10h) (IF_ADD_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

4.2.1 SPI read

Figure 7. **SPI read protocol**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

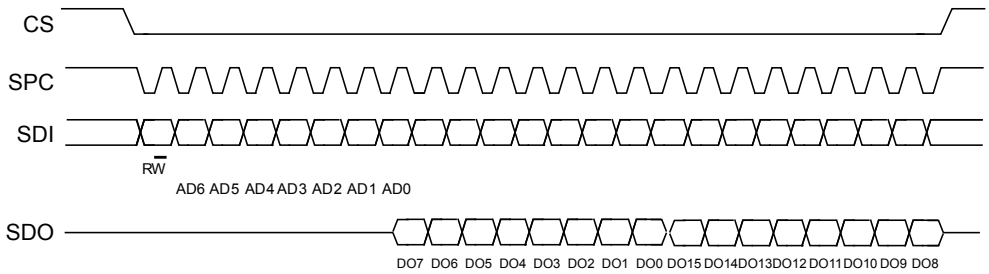
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

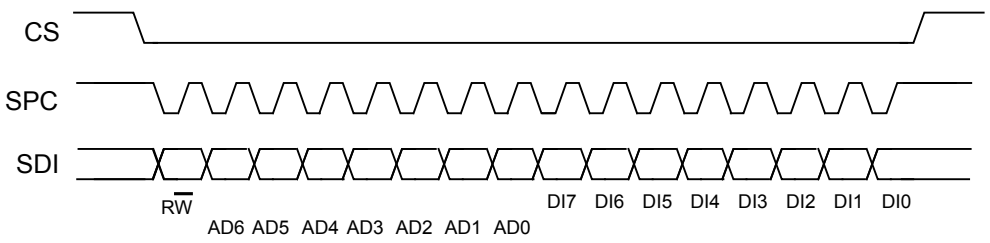
bit 16-... : data DO(...-8). Additional data in multiple byte reads.

Figure 8. **Multiple byte SPI read protocol (2-byte example)**



4.2.2 SPI write

Figure 9. **SPI write protocol**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

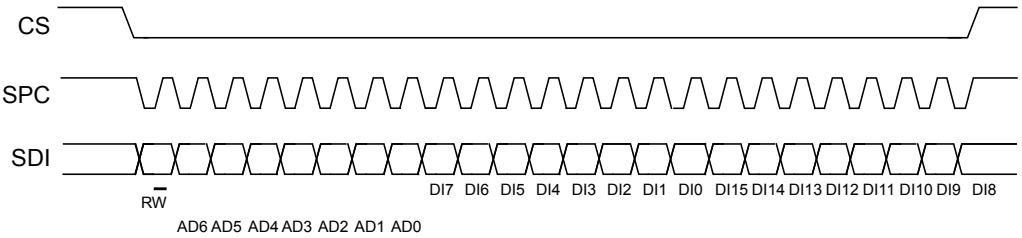
bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Additional data in multiple byte writes.

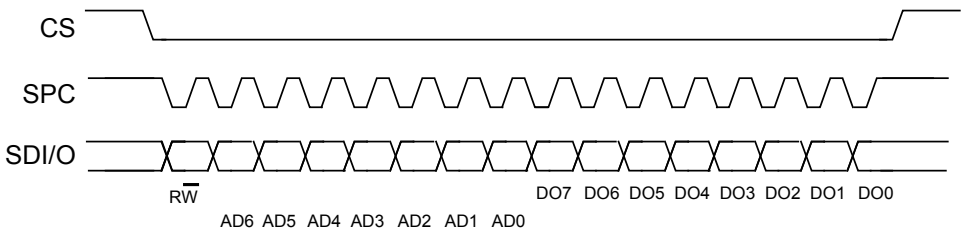
Figure 10. **Multiple byte SPI write protocol (2-byte example)**



4.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the PIN_CTRL (0Ch) (SIM) bit equal to 1 (SPI serial interface mode selection).

Figure 11. **SPI read protocol in 3-wire mode**



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

4.3 MIPI I3C® interface

4.3.1 MIPI I3C® target interface

The ST1VAFE3BX interface includes a MIPI I3C® SDR-only target interface able to work up to 12.5 MHz of the SCL frequency (compliant with release v1.1 of the specification) with MIPI I3C® SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-band interrupt request
- Target reset pattern for reset
- Error detection and recovery (S0 - S6)
- Group address

4.3.2 MIPI I3C® CCC supported commands

The list of MIPI I3C® CCC commands supported by the device is detailed in the following table.

Table 16. MIPI I3C® CCC commands

Command	Command code	Default	Description
ENTDAA	0x07		DAA procedure
SETDASA	0x87		Assign dynamic address using static address. Static address values are 0x18 / 0x19 depending on SDO pin.
ENEC	0x80 / 0x00		Target activity control (direct and broadcast)
DISEC	0x81/ 0x01		Target activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
RSTDAA	0x86(1) / 0x06		Reset the assigned dynamic address (direct(1) and broadcast)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B	0x00 0x08 (2 byte)	Get maximum write length during private write
GETMRL	0x8C	0x00 0x10 0x08 (3 byte)	Get maximum read length during private read
GETPID	0x8D	0x02 0x08 0x00 0x47 0x92 0x0B	SDO = 1
		0x02 0x08 0x00 0x47 0x12 0x0B	SDO = 0
GETBCR	0x8E	0x0F (1 byte)	Bus characteristics register
GETDCR	0x8F	0x41 default	MIPI I3C® device characteristics register
GETSTATUS	0x90	0x00 0x00 (2 byte)	Status register
GETMXDS	0x94	0x08 0x60 (2 byte)	Return max data speed
SETGRPA	0x9B		Group address assignment

Command	Command code	Default	Description
RSTGRPA	0x2C / 0x9C		Reset the group address
RSTACT(2)	0x9A / 0x2A		Configure target reset action
GETCAPS	0x95	0x00 0x11 0x18 0x00	Provide information about device capabilities and supported extended features

1. *Direct RSTDAA can be disabled by writing bit DIS_DRSTDAA in I3C_IF_CTRL (33h) to 1.*
2. *This command must be performed in power-down mode.*

4.3.3 Antispike filter management on mixed I²C/MIPI I3C® bus

In the ST1VAFE3BX, the SDA and SCL lines are common to both I²C and I3C. The I²C bus requires antispike filters on the SDA and SCL pins that are not compatible with I3C timing.

The device acts as a standard I²C target as long as it is in deep power-down or in soft power-down with an I²C static address.

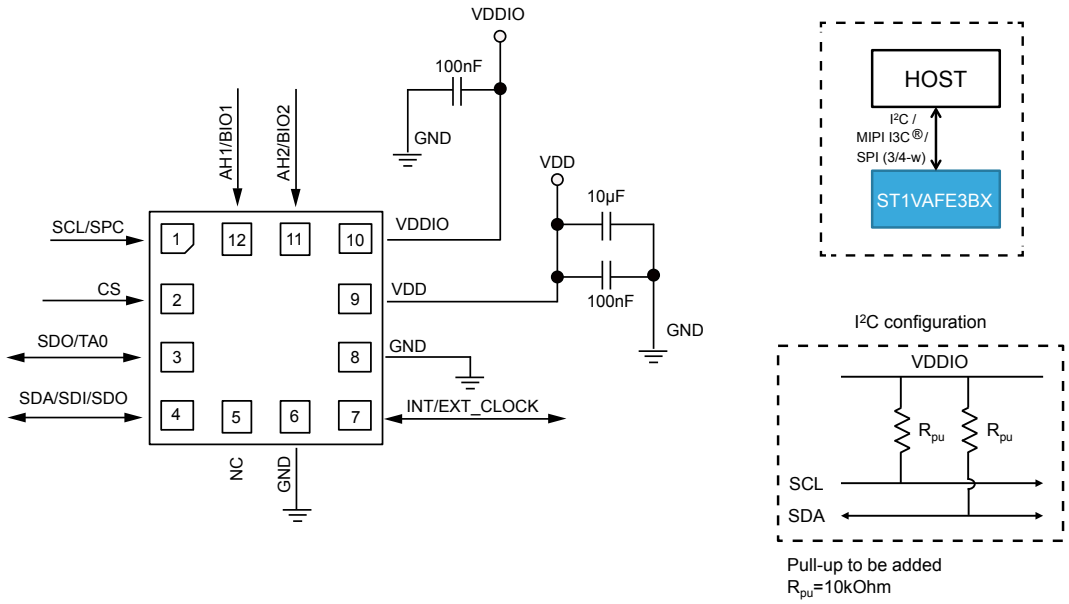
When in deep power-down, the controller must emit START, STATIC ADDRESS R/W (or dynamic address if previously assigned) at open-drain speed using I²C fast mode plus reference timing to perform a power-up command.

When the device is in soft power-down for the first time after a transition from the deep power-down state, the device is capable of detecting and disabling the I²C antispike filter after detecting the broadcast address (7'h7E/W). In order to guarantee proper behavior of the device, the I3C controller must emit the first START, 7'h7E/W at open-drain speed using I²C fast mode plus reference timing.

After detecting the broadcast address, the device can receive the I3C dynamic address following the I3C push-pull timing. If the device is not assigned a dynamic address, then it continues to operate as an I²C device with no antispike filter. For the case in which the host decides to keep the device as I²C with an antispike filter, there is a configuration required to keep the antispike filter active. This configuration is done by writing the ASF_ON bit to 1 in the I3C_IF_CTRL (33h) register. This configuration forces the antispike filter to always be turned on instead of being managed by the communication on the bus.

5 Application hints

Figure 12. **ST1VAFE3BX electrical connections (top view)**



The device core is supplied through the VDD line while the I/O pins are supplied through the VDDIO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to Figure 12). It is possible to remove VDD while maintaining VDDIO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data are selectable and accessible through the I²C/MIPI I3C® or SPI interfaces. When using the I²C, CS must be tied high (that is, connected to VDDIO).

The functions, the threshold and the timing of the interrupt pin (INT) can be completely programmed by the user through the I²C/MIPI I3C®/SPI interface.

ST1VAFE3BX electrical connections for the vAFE

The vAFE external electrode connections are illustrated in the following figure.

Figure 13. **vAFE external connections to pin 11, 12 (vAFE input)**

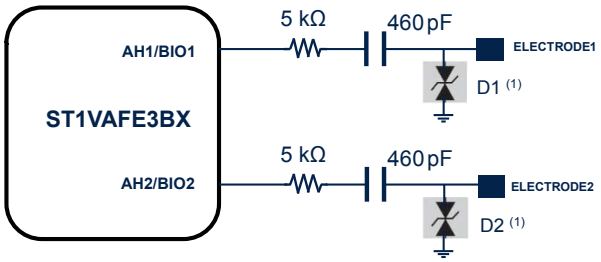


Table 17. Internal pin status

Pin #	Name	Function	Pin status
1	SCL SPC	I²C/MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)	Default: input without pull-up
2	CS	SPI/I²C/MIPI I3C® mode selection 1: SPI idle mode / I²C/MIPI I3C® enabled 0: SPI enabled / I²C/MIPI I3C® disabled	Default: input with internal pull-up
3	SDO TA0	Serial data output (SDO) I²C less significant bit of the device address (TA0)	Default: input without internal pull-up
4	SDA SDI SDO	I²C/MIPI I3C® serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	Default: (SDA) input without internal pull-up
5	NC	Internally not connected. Can be tied to VDD, VDDIO, or GND.	
6	GND	0 V supply	
7	INT/EXT_CLK	Connect to GND if not used as an interrupt pin(1) External clock for synchronization of multiple sensors. This pin has an internal pull-down connected until the INT_PIN_EN bit is set to 1 in register CTRL1 (10h)(2)	Default: input with internal pull-down
8	GND	0 V supply	
9	VDD	Power supply	
10	VDDIO	Power supply for I/O pins	
11	AH2/BIO2	AH input 2 (or BIO electrode 2)	Default: input with internal pull-down(3)
12	AH1/BIO1	AH input 1 (or BIO electrode 1)	Default: input with internal pull-down(3)

1. *When the interrupt flag in the CTRL2 (11h), MD1_CFG (1Fh), EMB_FUNC_INT (0Ah), FSM_INT (0Bh), and MLC_INT (0Dh) registers is set to 1, and the INT_PIN_EN bit of register CTRL1 (10h) is set to 1, the selected interrupt signals are routed to the INT pin.*
2. *When the external clock for the synchronization of multiple sensors is intended to be used, the EXT_CLK_EN bit must be set to 1 in register EXT_CLK_CFG (08h) and the bit INT_PIN_EN set to 0 in register CTRL1 (10h) in order to correctly drive the pin.*
3. *The internal pull-down is automatically disconnected when the power-up command is performed.*

6 Digital main blocks and embedded low-power features

The ST1VAFE3BX has been designed to be fully compliant with Android, featuring the following on-chip functions:

- FIFO data buffering
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable)
  - Free-fall
  - Wake-up
  - 6D/4D orientation
  - Single/double/triple-tap detection
  - Activity/inactivity recognition
  - Stationary/motion detection
- Specific IP blocks (called "embedded functions") with negligible power consumption and high-performance
  - Pedometer functions: step detector and step counters
  - Tilt
  - Significant motion detection
  - Finite state machine (FSM)
  - Machine learning core (MLC) with exportable features and filters for AI applications
  - Adaptive self-configuration (ASC)

6.1 FIFO

The ST1VAFE3BX embeds 128 slots of 7 bytes each (1 byte TAG + 6 bytes DATA). This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

FIFO is designed in order to allow the batching of different kinds of sensors. It is possible to store in FIFO the data of the accelerometer, and analog hub / vAFE physical sensors and the data of virtual sensors like the step counter, the MLC features / filters / results and FSM results.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO_DATA_OUT_TAG byte that allows recognizing the meaning of a word in FIFO.

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO dedicated configurations.

FIFO allows correctly reconstructing the timestamp information for each sensor stored in FIFO. Also, if a change in the ODR or BDR (batch data rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied in a FIFO stream without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

In order to maximize the amount of data collected in FIFO, it is possible to double the slots of FIFO data (from 128 to 256) by writing the FIFO_DEPTH bit to 1 in FIFO_CTRL (15h) with 2x depth mode. When this mode is enabled, the most significant 8 bits for each acceleration data are stored in FIFO. Each FIFO data word contains data of two consecutive ODRs, the actual and the previous one. 2x depth mode cannot be enabled in ultralow-power mode.

In high-resolution batch mode, accelerometer and analog hub / vAFE data are stored in FIFO in 12-bit format at the ODR rate.

In 2x depth batch mode, each FIFO word contains two accelerometer data in 8-bit format at the ODR/2 rate.

It is possible to avoid storing the AH / vAFE data in FIFO by setting the XL_ONLY_FIFO bit in the FIFO_WTM (16h) register to 1. In this case, the accelerometer data are stored in FIFO as 16-bit format at the ODR rate.

The FIFO buffer can work according to six different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous
- Bypass-to-FIFO

Each mode is selected by the FIFO_MODE[2:0] bits in the FIFO_CTRL (15h) register. A programmable FIFO watermark is selected in the FIFO_WTM (16h) register.

Continuous-to-FIFO mode, bypass-to-continuous mode, and bypass-to-FIFO mode are not available in the AH / vAFE only state.

The FIFO status is available in the FIFO_STATUS1 (26h) and FIFO_STATUS2 (27h) registers and can be used to generate dedicated interrupts on the INT pin using the CTRL2 (11h) register.

The FIFO_WTM_IA bit in the FIFO_STATUS1 (26h) register goes to 1 when the number of unread samples is greater than or equal to FTH[6:0] in FIFO_WTM (16h).

The FIFO_OVR_IA bit in FIFO_STATUS1 (26h) is equal to 1 if a FIFO sample is overwritten.

FSS[7:0] in FIFO_STATUS2 (27h) contains stored data levels of unread samples.

When FSS[7:0] is equal to 00000000, FIFO is empty. When FSS[7:0] is equal to 10000000, FIFO is full and the unread samples are 128.

6.1.1 Bypass mode

In bypass mode FIFO_CTRL (15h) (FIFO_MODE[2:0] = 000), the FIFO is not operational, the buffer content is cleared, and no data is collected in FIFO memory, which remains empty with only the actual sample available in the output registers.

Bypass mode is also used to reset the FIFO when in FIFO mode.

6.1.2 FIFO mode

In FIFO mode FIFO_CTRL (15h) (FIFO_MODE[2:0] = 001) data from the output channels are stored in the FIFO memory until it is full. When 128 unread samples are stored in memory, data collecting is stopped until FIFO mode is restarted.

To reset FIFO content, bypass mode should be selected by writing FIFO_CTRL (15h) (FIFO_MODE[2:0]) to 000. After this reset command, it is possible to restart FIFO mode, writing FIFO_CTRL (15h) (FIFO_MODE[2:0]) to 001.

6.1.3 Continuous mode

Continuous mode FIFO_CTRL (15h) (FIFO_MODE[2:0] = 110) provides a continuous FIFO update: when 128 unread samples are stored in memory, as new data arrives, the oldest data is discarded and overwritten by the newer.

A FIFO threshold flag FIFO_WTM_IA bit in FIFO_STATUS1 (26h) is asserted when the number of unread samples in FIFO is greater than or equal to FTH[6:0] in FIFO_WTM (16h).

It is possible to route the FIFO_WTM_IA bit to the INT pin by writing the INT_FIFO_TH bit to 1 in register CTRL2 (11h).

If an overrun occurs, the oldest sample in FIFO is overwritten and the FIFO_OVR_IA flag in FIFO_STATUS1 (26h) is asserted.

6.1.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode FIFO_MODE[2:0] = 011 in the FIFO_CTRL (15h) register, FIFO operates in continuous mode and FIFO mode starts upon an edge trigger event. When the FIFO is full, data collecting is stopped. The trigger event could be single/double/triple-tap, wake-up, free-fall, 6D interrupt or any combination of these events, but every interrupt has to be routed to the corresponding pin to be used as a trigger.

6.1.5 Bypass-to-continuous mode

In bypass-to-continuous mode FIFO_CTRL (15h) (FIFO_MODE[2:0] = 100), data measurement storage inside FIFO starts in continuous mode upon an edge trigger event.

The trigger event could be single/double/triple-tap, wake-up, free-fall, 6D interrupt or any combination of these events, but every interrupt has to be routed to the corresponding pin to be used as a trigger. The sample that generated the trigger is available in FIFO.

6.1.6 Bypass-to-FIFO

In bypass-to-FIFO mode FIFO_CTRL (15h)(FIFO_MODE_[2:0] = 111), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

The trigger event could be single/double/triple-tap, wake-up, free-fall, 6D interrupt or any combination of these events, but every interrupt has to be routed to the corresponding pin to be used as a trigger.

The sample that generated the trigger is available in FIFO.

6.1.7 FIFO reading procedure

When FIFO is enabled and the mode is different from bypass, reading the FIFO output registers return the oldest FIFO sample set. Whenever these registers are read, their content is moved to the SPI/I²C/MIPI I3C® output buffer.

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (FIFO_DATA_OUT_TAG (40h), in order to identify the sensor, and 6 bytes of fixed data (FIFO_DATA_OUT registers from (41h) to (46h)).

The FSS[7:0] field in the FIFO_STATUS2 (27h) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

Meta information about accelerometer configuration changes can be managed by enabling the CFG_CHG_EN bit in FIFO_CTRL (15h).

The entire FIFO content is retrieved by performing a certain number of read operations from the FIFO output registers until the buffer becomes empty (FSS[7:0] bits of the FIFO_STATUS2 (27h) register are equal to 0).

FIFO output data must be read with multiples of 7-byte reads starting from the FIFO_DATA_OUT_TAG (40h) register.

The rounding function (automatic wraparound) from address FIFO_DATA_OUT_Z_L (45h) and FIFO_DATA_OUT_Z_H (46h) to FIFO_DATA_OUT_TAG (40h) is done automatically in the device, in order to allow reading many words with a unique multiple read operation.

The recommended way to retrieve data from the FIFO is the following:

1. Read the FIFO_STATUS2 (27h) register to check how many words are stored in the FIFO. This information is contained in the FSS[7:0] bits.
2. For each word in FIFO, read the FIFO word (tag and output data) and interpret it on the basis of the FIFO tag.
3. Go to step 1.

6.1.8 FIFO empty condition

When FIFO is emptied, a dedicated FIFO tag value (equal to 00000) is used in order to recognize an empty condition and no duplicated samples are read. If samples are continuously read before a new sample arrives, the FIFO tag value continues to be equal to 00000.

6.2 Pedometer functions: step detector and step counters

The ST1VAFE3BX embeds an advanced pedometer with an algorithm running in an ultralow-power domain in order to ensure extensive battery life in battery-constrained applications.

Leveraging on enhanced configurability, the advanced embedded pedometer is suitable for a large range of applications from mobile to wearable devices.

The algorithm processes and analyzes the accelerometer waveform in order to count the user's steps during walking and running activities.

The pedometer works at 25 Hz and it is not affected by the selected device power mode (ultralow-power, low-power, high-performance), thus guaranteeing an ultralow-power experience and extreme flexibility in conjunction with other device functionalities.

The accelerometer operating mode can be changed at runtime and is based on user requirements without impacting the performance of the pedometer.

The pedometer output can be batched in the device's FIFO buffer, in order to decrease overall system supply current.

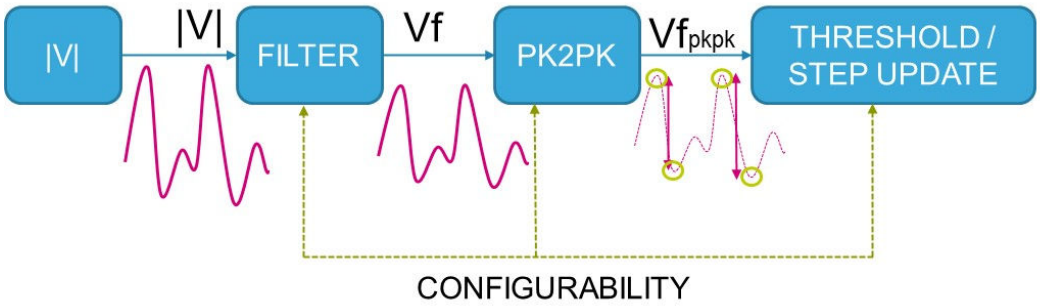
ST freely provides the support and the tools for easily configuring the device and tuning the algorithm configuration for a best-in-class user experience.

6.3 Pedometer algorithm

The pedometer algorithm is composed of a cascade of four stages:

1. Computation of the acceleration magnitude signal in order to detect the signal independently from device orientation;
2. FIR filter to extract relevant frequency components and to smooth the signal by cutting off high frequencies;
3. Peak detector to find the maximum and minimum of the waveform and compute the peak-to-peak value;
4. Step count: if the peak-to-peak value is greater than the settled threshold, a step is counted.

Figure 14. Four-stage pedometer algorithm



The ST1VAFE3BX embeds a dynamic internal threshold for step detection that is updated after each peak-to-peak evaluation: the internal threshold is increased with a configurable speed if a step is detected or decreased with a configurable speed if a step is not detected.

This approach ensures high accuracy when the user starts to walk and a false peak rejection when the user is walking or running.

An internal configurable debounce algorithm can be also set to filter false walks: indeed, an accelerometer pattern is recognized as a walk or run only if a minimum number of steps are counted.

The ST1VAFE3BX has been designed to reject a false-positive signal inside the algorithm core.

On top of the mechanisms detailed above, the ST1VAFE3BX allows enabling and configuring a dedicated false-positive rejection block to further boost pedometer accuracy.

6.4 Tilt detection

The tilt function helps to detect activity change and has been implemented in hardware using only the accelerometer to achieve targets of both ultralow power consumption and robustness during the short duration of dynamic accelerations.

The tilt function is based on a trigger of an event each time the device's tilt changes and can be used with different scenarios, for example:

- Triggers when the phone is in a front pants pocket and the user goes from sitting to standing or standing to sitting
- Does not trigger when the phone is in a front pants pocket and the user is walking, running, or going upstairs

6.5 Significant motion detection

The significant motion detection (SMD) function generates an interrupt when a ‘significant motion’, that could be due to a change in user location, is detected. In the ST1VAFE3BX device this function has been implemented in hardware using only the accelerometer.

SMD functionality can be used in location-based applications in order to receive a notification indicating when the user is changing location.

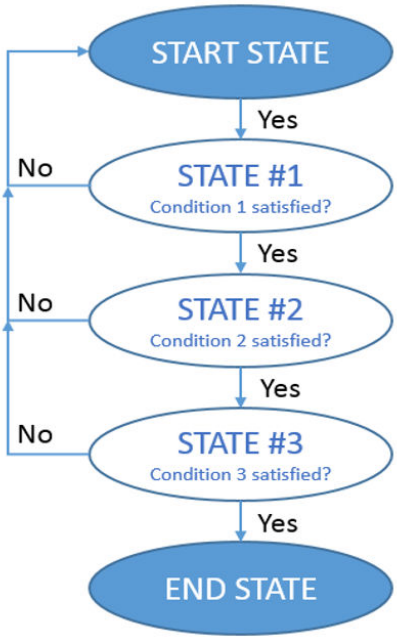
6.6 Finite state machine

The ST1VAFE3BX can be configured to generate interrupt signals activated by user-defined motion patterns. To do this, up to eight embedded finite state machines can be programmed independently for motion detection such as glance gestures, absolute wrist tilt, shake and double-shake detection.

Definition of finite state machine

A state machine is a mathematical abstraction used to design logic connections. It is a behavioral model composed of a finite number of states and transitions between states, similar to a flow chart in which one can inspect the way logic runs when certain conditions are met. The state machine begins with a start state, goes to different states through transitions dependent on the inputs, and can finally end in a specific state (called stop state). The current state is determined by the past states of the system. The following figure shows a generic state machine.

Figure 15. Generic state machine



Finite state machine in the ST1VAFE3BX

ST1VAFE3BX accelerometer data can be used as the input of up to eight programs in the embedded finite state machine (FSM); also the analog hub (AH) / vAFE data can be processed in FSM logic (Figure 16. State machine in the ST1VAFE3BX).

All eight finite state machines are independent: each one has its dedicated memory area and it is independently executed. An interrupt is generated when the end state is reached or when some specific command is performed.

Figure 16. State machine in the ST1VAFE3BX



6.7 Machine learning core

The ST1VAFE3BX embeds a dedicated core for machine learning processing that provides system flexibility, allowing some algorithms run in the application processor to be moved to the MEMS sensor with the advantage of consistent reduction in power consumption.

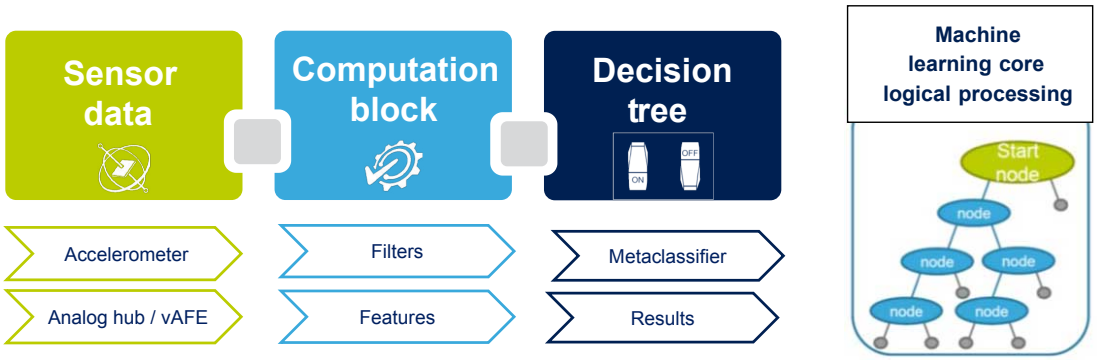
Machine learning core logic allows identifying if a data pattern matches a user-defined set of classes. Typical examples of applications could be activity detection like running, walking, driving, and so on.

The ST1VAFE3BX machine learning core works on data patterns coming from the accelerometer sensor, but it is also possible to process the analog hub (AH) / vAFE data.

The input data can be filtered using a dedicated configurable computation block containing filters and features computed in a fixed time window defined by the user. Computed feature values and filtered data values can also be read through the FIFO buffer.

Machine learning processing is based on logical processing composed of a series of configurable nodes characterized by "if-then-else" conditions where the "feature" values are evaluated against defined thresholds.

Figure 17. Machine learning core in the ST1VAFE3BX



The ST1VAFE3BX can be configured to run up to four decision trees simultaneously and independently and every decision tree can generate up to 16 results. The total number of nodes can be up to 128.

The results of the machine learning processing are available in dedicated output registers readable from the application processor at any time.

The ST1VAFE3BX machine learning core can be configured to generate an interrupt when a change in the result occurs.

6.8 Adaptive self-configuration (ASC)

The ST1VAFE3BX supports the adaptive self-configuration (ASC) feature, which allows the FSM to automatically reconfigure the device in real time based on the detection of a specific motion pattern or based on the output of a specific decision tree configured in the MLC, without any intervention from the host processor. The FSM can write a subset of the device registers using the SETR command, which allows indicating the register address and the new value to be written in such a register. The access to these device registers is mutually exclusive with respect to the host.

The ASC feature is not available in the AH / vAFE only state and cannot be used to toggle the AH_BIO_EN bit of the AH_BIO_CFG2 (31h) register.

7 Register mapping

The table given below provides a list of the 8-bit registers embedded in the device and the corresponding addresses.

Table 18. Register map

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
EXT_CLK_CFG	R/W	08	00001000	00000000	
PIN_CTRL	R/W	0C	00001100	00000000	
WAKE_UP_DUR_EXT	R/W	0E	00001110	00000000	
WHO_AM_I	R	0F	00001111	01001000	
CTRL1	R/W	10	00010000	00010000	
CTRL2	R/W	11	00010001	00000000	
CTRL3	R/W	12	00010010	00000000	
CTRL4	R/W	13	00010011	00000000	
CTRL5	R/W	14	00010100	00000000	
FIFO_CTRL	R/W	15	00010101	00000000	
FIFO_WTM	R/W	16	00010110	00000000	
INTERRUPT_CFG	R/W	17	00010111	00000000	
SIXD	R/W	18	00011000	00000000	
WAKE_UP_THS	R/W	1C	00011100	00000000	
WAKE_UP_DUR	R/W	1D	00011101	00000000	
FREE_FALL	R/W	1E	00011110	00000000	
MD1_CFG	R/W	1F	00011111	00000000	
WAKE_UP_SRC	R	21	00100001	00000000	
TAP_SRC	R	22	00100010	00000000	
SIXD_SRC	R	23	00100011	00000000	
ALL_INT_SRC	R	24	00100100	00000000	
STATUS	R	25	00100101	00000000	
FIFO_STATUS1	R	26	00100110	00000000	
FIFO_STATUS2	R	27	00100111	00000000	
OUT_X_L	R	28	00101000	00000000	
OUT_X_H	R	29	00101001	00000000	
OUT_Y_L	R	2A	00101010	00000000	
OUT_Y_H	R	2B	00101011	00000000	
OUT_Z_L	R	2C	00101100	00000000	
OUT_Z_H	R	2D	00101101	00000000	
OUT_AH_BIO_L	R	2E	00101110	00000000	
OUT_AH_BIO_H	R	2F	00101111	00000000	
AH_BIO_CFG1	R/W	30	00110000	00000000	
AH_BIO_CFG2	R/W	31	00110001	00000000	
AH_BIO_CFG3	R/W	32	00110010	00000000	

Name	Type[1]	Register address		Default	Comment
		Hex	Binary		
I3C_IF_CTRL	R/W	33	00110011	00000000	
EMB_FUNC_STATUS_MAINPAGE	R	34	00110100	00000000	
FSM_STATUS_MAINPAGE	R	35	00110101	00000000	
MLC_STATUS_MAINPAGE	R	36	00110110	00000000	
EN_DEVICE_CONFIG	W	3E	00111110	00000000	
FUNC_CFG_ACCESS	R/W	3F	00111111	00000000	
FIFO_DATA_OUT_TAG	R	40	01000000	00000000	
FIFO_DATA_OUT_X_L	R	41	01000001	00000000	
FIFO_DATA_OUT_X_H	R	42	01000010	00000000	
FIFO_DATA_OUT_Y_L	R	43	01000011	00000000	
FIFO_DATA_OUT_Y_H	R	44	01000100	00000000	
FIFO_DATA_OUT_Z_L	R	45	01000101	00000000	
FIFO_DATA_OUT_Z_H	R	46	01000110	00000000	
FIFO_BATCH_DEC	R/W	47	01000111	00000000	
TAP_CFG0	R/W	6F	01101111	00000000	
TAP_CFG1	R/W	70	01110000	00000000	
TAP_CFG2	R/W	71	01110001	00000000	
TAP_CFG3	R/W	72	01110010	00000000	
TAP_CFG4	R/W	73	01110011	00000000	
TAP_CFG5	R/W	74	01110100	00000000	
TAP_CFG6	R/W	75	01110101	00000000	
TIMESTAMP0	R	7A	01111010	00000000	
TIMESTAMP1	R	7B	01111011	00000000	
TIMESTAMP2	R	7C	01111100	00000000	
TIMESTAMP3	R	7D	01111101	00000000	

1. R = read-only register, R/W = readable/writable register

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

8.1 EXT_CLK_CFG (08h)

R/W

Table 19. Table 20. EXT_CLK_CFG register

EXT_CLK_EN	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 20. EXT_CLK_CFG register description

EXT_CLK_EN	If this bit is set to 1, the external oscillator, forced through the INT/EXT_CLK pin, replaces the internal oscillator. Default value: 0 Supported frequency 102.4 kHz ± 5%, supported duty cycle 50% ± 10%

8.2 PIN_CTRL (0Ch)

R/W

Table 21. Table 20. PIN_CTRL register

SDO_PU_EN	SDA_PU_EN	0(1)	0(1)	H_LACTIVE	CS_PU_DIS	PP_OD	SIM

1. *This bit must be set to 0 for the correct operation of the device.*

Table 22. PIN_CTRL register description

SDO_PU_EN	If 1, enables the internal pull-up of the SDO/TA0 pin.
SDA_PU_EN	If 1, enables the internal pull-up of the SDA/SDI/SDO pin.
H_LACTIVE	Interrupt active level (0: interrupts active-high (default); 1: Interrupts active-low)
CS_PU_DIS	If 1, disables the internal pull-up of the CS pin.
PP_OD	Push-pull/open-drain mode for INT pins (0: INT pins in push-pull mode (default); 1: INT pins in open-drain mode)
SIM	SPI 3 or 4-wire mode (0: 4-wire SPI (default); 1: 3-wire SPI)

8.3 WAKE_UP_DUR_EXT (0Eh)

R/W

Table 23. WAKE_UP_DUR_EXT register

0(1)	0(1)	0(1)	WU_DUR_EXTENDED	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 24. WAKE_UP_DUR_EXT register description

WU_DUR_EXTENDED	This bit is used to select the resolution of WAKE_DUR[1:0] bits in register WAKE_UP_DUR (1Dh). Default value: 0

8.4 WHO_AM_I (0Fh)

This register is a read-only register. Its value is fixed at 48h.

Table 25. WHO_AM_I register default values

0	1	0	0	1	0	0	0

8.5 CTRL1 (10h)

R/W

Table 26. CTRL1 register

SMART_POWER_EN	INT_PIN_EN	SW_RESET	IF_ADD_INC	DRDY_PULSED	WU_X_EN	WU_Y_EN	WU_Z_EN

Table 27. CTRL1 register description

SMART_POWER_EN	Enables smart power management when the embedded functions are enabled. Default value: 0 (0: disabled; 1: enabled)
INT_PIN_EN(1)	Enables routing the interrupt signals configured on the INT pin. Default value: 0 (0: disabled; 1: enabled)
SW_RESET	Software reset, resets all CTRL registers to their default values. Default value: 0 (0: disabled; 1: enabled) This bit is automatically reset to 0 at the end of the procedure.
IF_ADD_INC	The register address is automatically incremented during a multiple-byte access with a serial interface. (0: disabled; 1: enabled (default))
DRDY_PULSED	Enables pulsed data-ready mode (0: data-ready latched mode (returns to 0 only after reading over an interface) (default); 1: data-ready pulsed mode (the data-ready pulses are typ. 90 µs long))
WU_X_EN	Enables wake-up event detection status on the X-axis. Default value: 0 (0: disabled; 1: enabled)
WU_Y_EN	Enables wake-up event detection status on the Y-axis. Default value: 0 (0: disabled; 1: enabled)
WU_Z_EN	Enables wake-up event detection status on the Z-axis. Default value: 0 (0: disabled; 1: enabled)

1. *When the MIPI I3C® interface is used, this bit must be set to 0.*

8.6 CTRL2 (11h)

R/W

Table 28. CTRL2 register

INT_ BOOT	INT_FIFO _FULL	INT_FIFO _TH	INT_FIFO _OVR	INT_ DRDY	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 29. CTRL2 register description

INT_BOOT	Enables boot status on INT pin. Default value: 0 (0: disabled; 1: enabled)
INT_FIFO_FULL	Enables FIFO full on INT pin. Default value: 0 (0: disabled; 1: enabled)
INT_FIFO_TH	Enables FIFO threshold interrupt on INT pin. Default value: 0 (0: disabled; 1: enabled)
INT_FIFO_OVR	Enables overrun interrupt on INT pin. Default value: 0 (0: disabled; 1: enabled)
INT_DRDY	Data-ready interrupt on INT pin. Default value: 0 (0: disabled; 1: enabled)

8.7 CTRL3 (12h)

R/W

Table 30. CTRL3 register

0(1)	0(1)	0(1)	0(1)	0(1)	HP_EN	ST_SIGN_Y	ST_SIGN_X

1. *This bit must be set to 0 for the correct operation of the device.*

Table 31. CTRL3 register description

HP_EN(1)	If the device is not set in the AH / vAFE only state, this bit enables high-performance mode. Default value: 0 (0: low-power mode; 1: high-performance mode) If the device is set in the AH / vAFE only state (see Section 2.6: Analog hub / vAFE only state), this bit enables the LPF0 digital filter for the AH / vAFE chain. This is an FIR filter that performs 4 averages on AH / vAFE data, decimating the output data rate from 3200 Hz to 800 Hz. Default value: 0 (0: LPF0 filter off; 1: LPF0 filter on)
ST_SIGN_Y	Configures the sign of the self-test for the Y-axis. Default value: 0
ST_SIGN_X	Configures the sign of the self-test for the X-axis. Default value: 0

1. *The value of this bit can be changed in power-down mode only.*

8.8 CTRL4 (13h)

R/W

Table 32. CTRL4 register

INACT_ ODR1	INACT_ ODR0	BDU	EMB_FUNC _EN	FIFO_EN	0(1)	SOC	BOOT

1. *This bit must be set to 0 for the correct operation of the device.*

Table 33. CTRL4 register description

INACT_ODR[1:0]	If the activity/inactivity function is enabled, then these bits select the accelerometer ODR during inactivity status, see Table 34.
BDU	Sensing chain block data update(1) (0: output registers MSByte and LSByte independent continuous update (default); 1: output registers are not updated until MSByte and LSByte have both been read)
EMB_FUNC_EN	Enables embedded functions. To be set to 1 and to wait 5 ms before configuring the embedded functions. Default value: 0 (0: disabled; 1: enabled)
FIFO_EN	Enables batching in FIFO. To be set to 1 before configuring the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
SOC	Start of conversion bit. When one-shot mode using the interface (ODR[3:0] = 1111 in the CTRL5 (14h) register) is enabled, this bit provides the start for the measurement. This bit is automatically cleared.
BOOT	Reboots memory content. Default value: 0 (0: normal operating mode; 1: reboot memory content) This bit is automatically cleared. For proper execution of the boot procedure, set the device in high-performance mode.

1. *BDU is available in ultralow-power mode and low-power mode only.*

Table 34. ODR frequency in inactivity state

INACT_ODR1	INACT_ODR0	Frequency [Hz]
0	0	Stationary/motion detection: when selected, no ODR change is done if inactivity condition is detected (default)
0	1	1.6
1	0	3
1	1	25

8.9 CTRL5 (14h)

R/W

Table 35. CTRL5 register

ODR3	ODR2	ODR1	ODR0	BW1	BW0	FS1	FS0

Table 36. CTRL5 register description

ODR[3:0]	If the device is not set in the AH / vAFE only state, refer to the ODR selection in Table 37. If the device is set in the AH / vAFE only state (see Section 2.6: Analog hub / vAFE only state), refer to the ODR selection in Table 39.
BW[1:0]	If the device is not set in the AH / vAFE only state, these bits select the accelerometer bandwidth, which is dependent on the ODR selected. In high-performance mode (all ODR values) and in low-power mode for ODR ≥ 50 Hz, the available bandwidths are: ODR/2 (BW[1:0] = 00); ODR/4 (BW[1:0] = 01); ODR/8 (BW[1:0] = 10); ODR/16 (BW[1:0] = 11). In low-power mode for ODR < 50 Hz, refer to Table 38. If the device is set in the AH / vAFE only state (see Section 2.6: Analog hub / vAFE only state), these bits select the AH / vAFE sensor bandwidth, which is dependent on the ODR selected, see Table 39.
FS[1:0]	Sets the full scale, see Table 40.

Table 37. Operating modes

ODR[3:0]	Operating mode
0000	Power-down
0001	1.6 Hz in ultralow-power
0010	3 Hz in ultralow-power
0011	25 Hz in ultralow-power
0100	6 Hz
0101	12.5 Hz
0110	25 Hz
0111	50 Hz
1000	100 Hz
1001	200 Hz
1010	400 Hz
1011	800 Hz
1110	Reserved
1111	One-shot using the interface

Table 38. **Bandwidth selection (low-power mode with ODR < 50 Hz)**

ODR [Hz]	BW[1:0]	BW [Hz]
6	00	-
	01	-
	10	-
	11	3
12.5	00	-
	01	-
	10	6
	11	3
25	00	-
	01	12.5
	10	6
	11	3

Table 39. **Output data rate / bandwidth configurations in AH / vAFE only state**

ODR[3:0]	HP_EN	BW[1:0]	Output data rate	Bandwidth
0000	-	-	Power-down	-
1011	1	00	800 Hz	360
1011	1	01	800 Hz	180
1011	1	10	800 Hz	90
1011	1	11	800 Hz	45
1011	0	00	3200 Hz	1600
1011	0	01	3200 Hz	700
1011	0	10	3200 Hz	360
1011	0	11	3200 Hz	180

Table 40. **Full-scale selection**

FS1	FS0	Full scale
0	0	±2 *g*
0	1	±4 *g*
1	0	±8 *g*
1	1	±16 *g*

8.10 FIFO_CTRL (15h)

R/W

CFG_CHG_EN	FIFO_ DEPTH	0[1]	FIFO_EN_ADV	STOP_ON _FTH	FIFO_MODE2	FIFO_MODE1	FIFO_MODE0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 41. FIFO_CTRL register description

CFG_CHG_EN	Enables batching in FIFO of the device configuration and timestamp value when the ODR (output data rate) or the BDR (batch data rate) changes. Default value: 0 (0: disabled; 1: enabled)
FIFO_DEPTH	If 1, enables 2x depth mode for FIFO buffer.
FIFO_EN_ADV	This bit must be set to 1 when the embedded function results and/or the AH / vAFE data at 3200 Hz ODR are intended to be stored in FIFO. It can be set to 0 in the other cases. Default value: 0
STOP_ON_FTH	Sensing chain FIFO stop values memorization at threshold level. (0: FIFO depth is not limited (default); 1: FIFO depth is limited to threshold level)
FIFO_MODE[2:0][1]	Different FIFO modes are enabled as shown in Table 42.

1. *User must set the FIFO_EN bit to 1 in the CTRL4 (13h) register before setting the FIFO_MODE[2:0] bits.*

Table 42. Selection of FIFO mode

FIFO_MODE2	FIFO_MODE1	FIFO_MODE0	Mode
0	0	0	Bypass mode
0	0	1	FIFO mode: stops collecting data when FIFO is full
0	1	0	Reserved
0	1	1	Continuous-to-FIFO: stream mode until trigger is deasserted, then FIFO mode
1	0	0	Bypass-to-continuous: bypass mode until trigger is deasserted, then continuous mode
1	0	1	Reserved
1	1	0	Continuous mode: if the FIFO is full, the new sample overwrites the older sample.
1	1	1	Bypass-to-FIFO: bypass mode until trigger is deasserted, then FIFO mode

8.11 FIFO_WTM (16h)

R/W

Table 43. FIFO_WTM register

XL_ONLY _FIFO	FTH6	FTH5	FTH4	FTH3	FTH2	FTH1	FTH0

Table 44. FIFO_WTM register description

XL_ONLY_FIFO	FIFO data configuration. If this bit is set to 0 (default), accelerometer data and AH / vAFE data are stored in FIFO. If this bit is set to 1, only accelerometer data are stored in FIFO.
FTH[6:0]	FIFO watermark threshold, maximum value is 127.

8.12 INTERRUPT_CFG (17h)

R/W

Table 45. INTERRUPT_CFG register

TIMESTAMP _EN	0(1)	WAKE_ THS_W	0(1)	SLEEP_STAT US_ON_INT	DIS_RST_LIR _ALL_INT	LIR	INTERRUPTS _ENABLE

1. *This bit must be set to 0 for the correct operation of the device.*

Table 46. INTERRUPT_CFG register description

TIMESTAMP_EN	Enables timestamp counter. The counter is readable in TIMESTAMP0 (7Ah), TIMESTAMP1 (7Bh), TIMESTAMP2 (7Ch), and TIMESTAMP3 (7Dh). Default value: 0 (0: disabled; 1: enabled)
WAKE_THS_W	Weight of 1 LSB of wake-up threshold. Default value: 0 (0: 1 LSB = FS_XL / (2^6); 1: 1 LSB = FS_XL / (2^8))
SLEEP_STATUS_ON_INT	Sends the sleep status instead of sleep change to the INT pin (only if the INT_SLEEP_CHANGE bit is enabled, in register MD1_CFG (1Fh)). Default value: 0 (0: sleep change on INT pin; 1: sleep status on INT pin)
DIS_RST_LIR_ALL_INT	If 1, disables the reset of the interrupt flags when ALL_INT_SRC (24h) is read.
LIR	Interrupt mode configuration (see Table 2). Default value: 0 (0: interrupt level mode; 1: interrupt latched mode)
INTERRUPTS_ ENABLE	Enables basic interrupts (6D/4D, free-fall, wake-up, single/double/triple-tap, activity/inactivity). Default value: 0 (0: interrupt disabled; 1: interrupt enabled)

8.13 SIXD (18h)

R/W

Table 47. SIXD register

D4D_EN	D6D_THS1	D6D_THS0	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 48. SIXD register description

D4D_EN	Enables 4D orientation detection. Z-axis position detection is disabled. Default value: 0 (0: disabled; 1: enabled)
D6D_THS[1:0]	Thresholds for 4D/6D function (00: 80 degrees (default); 01: 70 degrees; 10: 60 degrees; 11: 50 degrees)

8.14 WAKE_UP_THS (1Ch)

R/W

Table 49. WAKE_UP_THS register

0 (1)	SLEEP_ ON	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 50. WAKE_UP_THS register description

SLEEP_ON	If 1, activity/inactivity function is enabled.
WK_THS[5:0]	Threshold for wake-up: 1 LSB weight depends on WAKE_THS_W in INTERRUPT_CFG (17h). Default value: 000000

8.15 WAKE_UP_DUR (1Dh)

R/W

Table 51. WAKE_UP_DUR register

FF_DUR5	WAKE_ DUR1	WAKE_ DUR0	ST_SIGN_Z	SLEEP_ DUR3	SLEEP_ DUR2	SLEEP_ DUR1	SLEEP_ DUR0

Table 52. WAKE_UP_DUR register description

FF_DUR5	Free-fall duration. Default value: 0 In conjunction with FF_DUR[4:0] in FREE_FALL (1Eh). 1 LSB: 1 ODR_period
WAKE_DUR[1:0]	Wake-up duration. Default value: 00 When the WU_DUR_EXTENDED bit in register WAKE_UP_DUR_EXT (0Eh) is set to 0, 1LSB of WAKE_DUR = 1 ODR_period, otherwise the following durations are selectable: (00: 3 ODR_period; 01: 7 ODR_period; 10: 11 ODR_period; 11: 15 ODR_period)
ST_SIGN_Z	Configures the sign of the self-test for the Z-axis. Default value: 0
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 which corresponds to 16 ODR_period 1 LSB: 512 ODR_period

8.16 FREE_FALL (1Eh)

R/W

Table 53. FREE_FALL register

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0

Table 54. FREE_FALL register description

FF_DUR[4:0]	Free-fall duration. Default value: 0 In conjunction with FF_DUR5 in WAKE_UP_DUR (1Dh) 1 LSB: 1 ODR_period
FF_THS[2:0]	Free-fall threshold (000: 156 mg; 001: 219 mg; 010: 250 mg; 011: 312 mg; 100: 344 mg; 101: 406 mg; 110: 469 mg; 111: 500 mg)

8.17 MD1_CFG (1Fh)

R/W

Each bit in this register enables a signal to be carried over the INT pin; the pin's output is the OR combination of the signals selected here and in register CTRL2 (11h).

Table 55. MD1_CFG register

INT_ SLEEP CHANGE	0(1)	INT_WU	INT_FF	INT_TAP	INT_6D	INT_ TIMESTAMP	INT_EMB _FUNC

1. *This bit must be set to 0 for the correct operation of the device.*

Table 56. MD1_CFG register description

INT_SLEEP_CHANGE	Enables sleep change (or sleep status, depending on the SLEEP_STATUS_ON_INT bit) on the INT pin.
INT_WU	Enables routing a wake-up event to the INT pin.
INT_FF	Enables routing a free-fall event to the INT pin.
INT_TAP	Enables routing a tap event to the INT pin.
INT_6D	Enables routing a 6D recognition event to the INT pin.
INT_TIMESTAMP	Enables routing the alert of a timestamp overflow within 2.5 ms to the INT pin.
INT_EMB_FUNC	Enables routing an embedded functions event to the INT pin.

8.18 WAKE_UP_SRC (21h)

R

Table 57. WAKE_UP_SRC register

-	SLEEP_ CHANGE_IA	FF_IA	SLEEP_ STATE	WU_IA	X_WU	Y_WU	Z_WU

Table 58. WAKE_UP_SRC register description

SLEEP_CHANGE_IA	Detection of change in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
FF_IA	Free-fall event detection status. Default value: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE	Sleep status bit. Default value: 0 (0: activity status; 1: inactivity status)
WU_IA	Wake-up event detection status. Default value: 0 (0: wake-up event not detected; 1: wake-up event detected)
X_WU	Wake-up event detection status on X-axis. Default value: 0 (0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected)
Y_WU	Wake-up event detection status on Y-axis. Default value: 0 (0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected)
Z_WU	Wake-up event detection status on Z-axis. Default value: 0 (0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected)

8.19 TAP_SRC (22h)

R

Table 59. **TAP_SRC register**

TAP_IA	SINGLE_ TAP_IA	DOUBLE_ TAP_IA	TRIPLE_ TAP_IA	-	-	-	-

Table 60. **TAP_SRC register description**

TAP_IA	Tap event detection status. Default: 0 (0: tap event not detected; 1: tap event detected)
SINGLE_TAP_IA	Single-tap event status. Default value: 0 (0: single-tap event not detected; 1: single-tap event detected)
DOUBLE_TAP_IA	Double-tap event detection status. Default value: 0 (0: double-tap event not detected; 1: double-tap event detected)
TRIPLE_TAP_IA	Triple-tap event detection status. Default value: 0 (0: triple-tap event not detected; 1: triple-tap event detected)

8.20 SIXD_SRC (23h)

R

Table 61. **SIXD_SRC register**

-	D6D_IA	ZH	ZL	YH	YL	XH	XL

Table 62. **SIXD_SRC register description**

D6D_IA	Source of change in 6D/4D orientation. Default value: 0 (0: change orientation not detected; 1: change orientation detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over-threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

8.21 ALL_INT_SRC (24h)

R

Table 63. ALL_INT_SRC register

-	SLEEP_ CHANGE_IA_ALL	D6D_ IA_ALL	TRIPLE_ TAP_ALL	DOUBLE_ TAP_ALL	SINGLE_ TAP_ALL	WU_IA_ ALL	FF_IA_ ALL

Table 64. ALL_INT_SRC register description

SLEEP_CHANGE_IA_ALL	Detection of change in activity/inactivity status. Default value: 0 (0: change in status not detected; 1: change in status detected)
D6D_IA_ALL	Source of change in 6D/4D orientation. Default value: 0 (0: change in orientation not detected; 1: change in orientation detected)
TRIPLE_TAP_ALL	Triple-tap event status. Default value: 0 (0: event not detected, 1: event detected)
DOUBLE_TAP_ALL	Double-tap event status. Default value: 0 (0: event not detected, 1: event detected)
SINGLE_TAP_ALL	Single-tap event status. Default value: 0 (0: event not detected, 1: event detected)
WU_IA_ALL	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)
FF_IA_ALL	Free-fall event status. Default value: 0 (0: event not detected, 1: event detected)

8.22 STATUS (25h)

R

Table 65. STATUS register

-	-	INT_GLOBAL	-	-	-	-	DRDY

Table 66. STATUS register description

INT_GLOBAL	This bit is 1 if one of the following events occurs: • detection of change in activity/inactivity status • source of change in 6D/4D orientation • single/double/triple-tap event status • wake-up event detection status • free-fall event detection status • sleep event status
DRDY	This bit is set to 1 when a new set of data samples is available and until the MSB of one of the output registers has been read.

8.23 FIFO_STATUS1 (26h)

R

Table 67. **FIFO_STATUS1 register**

FIFO_ WTM_IA	FIFO_ OVR_IA	-	-	-	-	-	-

Table 68. **FIFO_STATUS1 register description**

FIFO_WTM_IA	FIFO watermark status. The watermark is set through bits FTH[6:0] in FIFO_WTM (16h). (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or higher than WTM)
FIFO_OVR_IA	FIFO overrun status: 1 if FIFO has overwritten data.

8.24 FIFO_STATUS2 (27h)

R

Table 69. **FIFO_STATUS2 register**

FSS7	FSS6	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

Table 70. **FIFO_STATUS2 register description**

FSS[7:0]	Number of unread data stored in FIFO

8.25 OUT_X_L (28h)

R

Table 71. **OUT_X_L register**

OUTX7	OUTX6	OUTX5	OUTX4	OUTX3	OUTX2	OUTX1	OUTX0

Table 72. **OUT_X_L register description**

OUTX[7:0]	LSBs of X data output

8.26 OUT_X_H (29h)

R

Table 73. **OUT_X_H register**

OUTX15	OUTX14	OUTX13	OUTX12	OUTX11	OUTX10	OUTX9	OUTX8

Table 74. **OUT_X_H register description**

OUTX[15:8]	MSBs of X data output

8.27 OUT_Y_L (2Ah)

R

Table 75. **OUT_Y_L register**

OUTY7	OUTY6	OUTY5	OUTY4	OUTY3	OUTY2	OUTY1	OUTY0

Table 76. **OUT_Y_L register description**

OUTY[7:0]	LSBs of Y data output

8.28 OUT_Y_H (2Bh)

R

Table 77. **OUT_Y_H register**

OUTY15	OUTY14	OUTY13	OUTY12	OUTY11	OUTY10	OUTY9	OUTY8

Table 78. **OUT_Y_H register description**

OUTY[15:8]	MSBs of Y data output.

8.29 OUT_Z_L (2Ch)

R

Table 79. **OUT_Z_L register**

OUTZ7	OUTZ6	OUTZ5	OUTZ4	OUTZ3	OUTZ2	OUTZ1	OUTZ0

Table 80. **OUT_Z_L register description**

OUTZ[7:0]	LSBs of Z data output

8.30 OUT_Z_H (2Dh)

R

Table 81. **OUT_Z_H register**

OUTZ15	OUTZ14	OUTZ13	OUTZ12	OUTZ11	OUTZ10	OUTZ9	OUTZ8

Table 82. **OUT_Z_H register description**

OUTZ[15:8]	MSBs of Z data output

8.31 OUT_AH_BIO_L (2Eh)

R

Table 83. OUT_AH_BIO_L register

OUT_ AH_BIO7	OUT_ AH_BIO6	OUT_ AH_BIO5	OUT_ AH_BIO4	OUT_ AH_BIO3	OUT_ AH_BIO2	OUT_ AH_BIO1	OUT_ AH_BIO0

Table 84. OUT_AH_BIO_L register description

OUT_AH_BIO[7:0]	LSB of AH / vAFE data output

8.32 OUT_AH_BIO_H (2Fh)

R

Table 85. OUT_AH_BIO_H register

OUT_ AH_BIO15	OUT_ AH_BIO14	OUT_ AH_BIO13	OUT_ AH_BIO12	OUT_ AH_BIO11	OUT_ AH_BIO10	OUT_ AH_BIO9	OUT_ AH_BIO8

Table 86. OUT_AH_BIO_H register description

OUT_AH_BIO[15:8]	MSB of AH / vAFE data output

8.33 AH_BIO_CFG1 (30h)

R/W

Table 87. AH_BIO_CFG1 register

0(1)	0(1)	0(1)	AH_BIO_ZIN_ DIS_AH2_BIO2	AH_BIO_ZIN_ DIS_AH2_BIO1	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 88. AH_BIO_CFG1 register description

AH_BIO_ZIN_DIS_AH2_BIO2	Disables switching the AH2/BIO2 pin impedance. Default: 0 (0: switching enabled; 1: switching disabled)
AH_BIO_ZIN_DIS_AH2_BIO1	Disables switching the AH1/BIO1 pin impedance. Default: 0 (0: switching enabled; 1: switching disabled)

8.34 AH_BIO_CFG2 (31h)

R/W

Table 89. AH_BIO_CFG2 register

0(1)	AH_BIO_ MODE1	AH_BIO_ MODE0	AH_BIO_ C_ ZIN1	AH_BIO_ C_ZIN0	AH_BIO_ GAIN1	AH_BIO_ GAIN0	AH_BIO_ EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 90. AH_BIO_CFG2 register description

AH_BIO_MODE[1:0]	Selects differential / single-ended mode or resets the input of the AH / vAFE channel to common mode: (00: differential mode (default); 01: single-ended mode - input 2 is grounded, input 1 is connected to the AH / vAFE channel; 10: single-ended mode - input 1 is grounded, input 2 is connected to the AH / vAFE channel; 11: forced reset - the inputs are forced to common-mode voltage)
AH_BIO_C_ZIN[1:0]	Configures the equivalent input impedance of the AH / vAFE channel: (00: 100 MOhm (default); 01: 200 MOhm; 10: 500 MOhm; 11: 1 GOhm)
AH_BIO_GAIN[1:0]	Configures the AH / vAFE input/output gain: (00: 2 (default); 01: 4; 10: 8; 11: 16)
AH_BIO_EN(1)	Enables the AH / vAFE only state (see Section 2.6: Analog hub / vAFE only state).

1. *The value of this bit can be changed in power-down mode only.*

8.35 AH_BIO_CFG3 (32h)

R/W

Table 91. AH_BIO_CFG3 register

0(1)	0(1)	ST1	ST0	0(1)	0(1)	0(1)	AH_BIO_ ACTIVE

1. *This bit must be set to 0 for the correct operation of the device.*

Table 92. AH_BIO_CFG3 register description

ST[1:0]	These bits enable data acquisition during the self-test procedure.
AH_BIO_ACTIVE	This bit must only be used in the procedure to set the device in active mode when it is set in the AH / vAFE only state (see Section 2.6: Analog hub / vAFE only state), otherwise to be set to 0.

8.36 I3C_IF_CTRL (33h)

R/W

Table 93. I3C_IF_CTRL register

DIS_ DRSTDAA	0(1)	ASF_ON	0(1)	0(1)	0(1)	BUS_ACT_ SEL_1	BUS_ACT_ SEL_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 94. I3C_IF_CTRL register description

DIS_DRSTDAA	If 0, direct RSTDAA is supported. If 1, direct RSTDAA is disabled.
ASF_ON	If 1, enables the antispike filter even if the dynamic address is assigned.
BUS_ACT_SEL_[1:0]	Bus available time selection for IBI (in-band interrupt): (00: 20 µs; 01: 50 µs (default); 10: 1 ms; 11: 25 ms)

8.37 EMB_FUNC_STATUS_MAINPAGE (34h)

R

Table 95. EMB_FUNC_STATUS_MAINPAGE register

IS_FSM_LC	0	IS_SIGMOT	IS_TILT	IS_STEP_DET	0	0	0

Table 96. EMB_FUNC_STATUS_MAINPAGE register description

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)
IS_SIGMOT	Interrupt status bit for significant motion detection. (1: interrupt detected; 0: no interrupt)
IS_TILT	Interrupt status bit for tilt detection. (1: interrupt detected; 0: no interrupt)
IS_STEP_DET	Interrupt status bit for step detection. (1: interrupt detected; 0: no interrupt)

8.38 FSM_STATUS_MAINPAGE (35h)

R

Table 97. FSM_STATUS_MAINPAGE register

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1

Table 98. FSM_STATUS_MAINPAGE register description

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

8.39 MLC_STATUS_MAINPAGE (36h)

R

Table 99. MLC_STATUS_MAINPAGE register

0	0	0	0	IS_MLC4	IS_MLC3	IS_MLC2	IS_MLC1

Table 100. MLC_STATUS_MAINPAGE register description

IS_MLC4	Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC3	Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC2	Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC1	Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt)

8.40 EN_DEVICE_CONFIG (3Eh)

W

Table 101. EN_DEVICE_CONFIG register

-	-	-	-	-	-	-	EN_DEV_CONF

Table 102. EN_DEVICE_CONFIG register description

EN_DEV_CONF	Enables the configuration of the device when the SPI interface is used. The registers are not accessible until this bit is written.

8.41 FUNC_CFG_ACCESS (3Fh)

Enable embedded functions register (R/W)

Table 103. FUNC_CFG_ACCESS register

EMB_FUNC_ REG_ACCESS	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	FSM_WR_ CTRL_EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 104. FUNC_CFG_ACCESS register description

EMB_FUNC_REG_ACCESS	Enables access to the embedded functions registers.(1) Default value: 0 (0: disabled; 1: enabled)
FSM_WR_CTRL_EN	Enables the FSM to control the CTRL registers (the FSM can change some configurations of the device autonomously). Default value: 0 (0: disabled; 1: enabled)

1. *Details concerning the embedded functions registers are available in Section 9: Embedded functions register mapping and Section 10: Embedded functions register description.*

8.42 FIFO_DATA_OUT_TAG (40h)

This register contains the TAG values that distinguish the different kinds of data that can be batched in FIFO (R).

Table 105. FIFO_DATA_OUT_TAG register

TAG_ SENSOR_4	TAG_ SENSOR_3	TAG_ SENSOR_2	TAG_ SENSOR_1	TAG_ SENSOR_0	0	0	-

Table 106. FIFO_DATA_OUT_TAG register description

TAG_SENSOR_[4:0]	FIFO tag. Identifies the sensor in FIFO_DATA_OUT_X_L (41h) and FIFO_DATA_OUT_X_H (42h), FIFO_DATA_OUT_Y_L (43h) and FIFO_DATA_OUT_Y_H (44h), and FIFO_DATA_OUT_Z_L (45h) and FIFO_DATA_OUT_Z_H (46h). For details, refer to Table 107.

Table 107. Identification of sensor in FIFO

TAG_SENSOR_[4:0]	Data in FIFO
00000	FIFO empty
00010	Only accelerometer data
00011	Only accelerometer data (2x depth mode)
00100	Timestamp or CFG_CHG
10010	Step counter
11010	MLC result
11011	MLC filter
11100	MLC feature
11101	FSM result
11110	Analog hub / vAFE data in the AH / vAFE only state
11111	Accelerometer and analog hub / vAFE

8.43 FIFO_DATA_OUT_X_L (41h) and FIFO_DATA_OUT_X_H (42h)

FIFO data output X (R)

Table 108. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 109. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L register description

D[15:0]	FIFO X-axis output

8.44 FIFO_DATA_OUT_Y_L (43h) and FIFO_DATA_OUT_Y_H (44h)

FIFO data output Y (R)

Table 110. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 111. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L register description

D[15:0]	FIFO Y-axis output

8.45 FIFO_DATA_OUT_Z_L (45h) and FIFO_DATA_OUT_Z_H (46h)

FIFO data output Z (R)

Table 112. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L registers

D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 113. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L register description

D[15:0]	FIFO Z-axis output

8.46 FIFO_BATCH_DEC (47h)

R/W

Table 114. **FIFO_BATCH_DEC register**

0	0	0	DEC_TS_ BATCH_1	DEC_TS_ BATCH_0	BDR_XL_2	BDR_XL_1	BDR_XL_0

Table 115. **FIFO_BATCH_DEC register description**

DEC_TS_BATCH_[1:0]	Selects decimation for timestamp batching in FIFO. The write rate is the accelerometer BDR divided by the decimation decoder. (00: Timestamp not batched in FIFO (default); 01: Decimation 1: BDR_XL[Hz]; 10: Decimation 8: BDR_XL[Hz]/8 [Hz]; 11: Decimation 32: BDR_XL[Hz]/32 [Hz])
BDR_XL_[2:0]	Selects the batch data rate (write frequency in FIFO) for accelerometer data, see Table 116.

Table 116. **Accelerometer batch data rate**

BDR_XL_[2:0]	Accelerometer batch frequency
000	ODR (default)
001	ODR/2
010	ODR/4
011	ODR/8
100	ODR/16
101	ODR/32
110	ODR/64
111	Accelerometer not batched in FIFO

8.47 TAP_CFG0 (6Fh)

R/W

Table 117. TAP_CFG0 register

AXIS1	AXIS0	INVERT_T4	INVERT_T3	INVERT_T2	INVERT_T1	INVERT_T0	-

Table 118. TAP_CFG0 register description

AXIS[1:0]	Selection of axis for tap event research: (00: no axis (default); 01: X-axis; 10: Y-axis; 11: Z-axis)
INVERT_T[4:0]	These bits enable the search of the inverted peak by selecting the maximum number of samples between the first and second (inverted) peak in tap detection. (0: disabled) 1 LSB = 1 sample (maximum 31 samples)

8.48 TAP_CFG1 (70h)

R/W

Table 119. TAP_CFG1 register

PRE_STILL _THS3	PRE_STILL _THS2	PRE_STILL _THS1	PRE_STILL _THS0	POST_STILL _T3	POST_STILL _T2	POST_STILL _T1	POST_STILL _T0

Table 120. TAP_CFG1 register description

PRE_STILL_THS[3:0][1]	Threshold for stationary condition before shock. 1 LSB = 62.5 mg (maximum 937.5 mg)
POST_STILL_T[3:0]	Number of samples during stationary condition after shock and wait phases. These bits are used together with POST_STILL_T[5:4] in register TAP_CFG2 (71h). 1 LSB = 4 samples (maximum 252 samples).

1. *The PRE_STILL_THS[3:0] field must be set to a value greater than 0.*

8.49 TAP_CFG2 (71h)

R/W

Table 121. TAP_CFG2 register

POST_STILL_T5	POST_STILL_T4	WAIT_T5	WAIT_T4	WAIT_T3	WAIT_T2	WAIT_T1	WAIT_T0

Table 122. TAP_CFG2 register description

POST_STILL_T[5:4]	Number of samples during stationary condition after shock and wait phases. These bits are used together with POST_STILL_T[3:0] in register TAP_CFG1 (70h). 1 LSB = 4 samples (maximum 252 samples).
WAIT_T[5:0]	These bits program the number of samples to wait for the shock to finish. 1 LSB = 2 samples (maximum 126 samples).

8.50 TAP_CFG3 (72h)

R/W

Table 123. TAP_CFG3 register

POST_STILL_THS3	POST_STILL_THS2	POST_STILL_THS1	POST_STILL_THS0	LATENCY_T3	LATENCY_T2	LATENCY_T1	LATENCY_T0

Table 124. TAP_CFG3 register description

POST_STILL_THS[3:0](1)	Threshold for stationary condition after shock and wait phases. 1 LSB = 62.5 mg (maximum 937.5 mg)
LATENCY_T[3:0]	Maximum number of samples between consecutive taps event to detect double or triple tap. The default value of these bits is 0000b which corresponds to 16 samples. If the LATENCY_T[3:0] bits are set to a different value, 1LSB corresponds to 32 samples (maximum 480 samples).

1. *The POST_STILL_THS[3:0] field must be set to a value greater than 0.*

8.51 TAP_CFG4 (73h)

R/W

Table 125. TAP_CFG4 register

WAIT_END_LATENCY	0	PEAK_THS5	PEAK_THS4	PEAK_THS3	PEAK_THS2	PEAK_THS1	PEAK_THS0

Table 126. TAP_CFG4 register description

WAIT_END_LATENCY	This bit enables the feature to wait for the end of the latency window to exclusively determine if the event is a single, double or triple tap. (0: tap event flag is raised immediately for every detected tap; 1: in case of consecutive taps, only the flag for the highest level of tap is raised. The tap event flag is raised immediately if the highest level of tap enabled in TAP_CFG5 (74h) (single, double or triple) is reached, otherwise it is raised at the end of the latency window if no additional taps are detected within the window.)
PEAK_THS[5:0]	Threshold for peak detection. 1 LSB = 62.5 mg (maximum 3937.5 mg)

8.52 TAP_CFG5 (74h)

R/W

Table 127. **TAP_CFG5 register**

TRIPLE_TAP_EN	DOUBLE_TAP_EN	SINGLE_TAP_EN	REBOUND_T4	REBOUND_T3	REBOUND_T2	REBOUND_T1	REBOUND_T0

Table 128. **TAP_CFG5 register description**

TRIPLE_TAP_EN	This bit enables the triple-tap event. Default value: 0 (0: disabled; 1: enabled)
DOUBLE_TAP_EN	This bit enables the double-tap event. Default value: 0 (0: disabled; 1: enabled)
SINGLE_TAP_EN	This bit enables the single-tap event. Default value: 0 (0: disabled; 1: enabled)
REBOUND_T[4:0]	These bits program the number of samples to wait for the rebound to finish. The default value of these bits is 00000b which means that the rebound logic is disabled. If the REBOUND_T[4:0] bits are set to a different value, 1LSB corresponds to 2 samples (maximum 62 samples).

8.53 TAP_CFG6 (75h)

R/W

Table 129. **TAP_CFG6 register**

PRE_STILL_ST3	PRE_STILL_ST2	PRE_STILL_ST1	PRE_STILL_ST0	PRE_STILL_N3	PRE_STILL_N2	PRE_STILL_N1	PRE_STILL_N0

Table 130. **TAP_CFG6 register description**

PRE_STILL_ST[3:0]	Selection of starting sample for stationary condition before shock (from the oldest sample in a buffer of 14 samples). 1 LSB = 1 sample (0: 1st sample, 13: 14th sample, maximum value is 13)
PRE_STILL_N[3:0]	Selection of number of samples for stationary condition before shock. 1 LSB = 1 sample (maximum 14 samples). If this field is set to 0, the stationary condition before shock is disabled.

8.54 TIMESTAMP0 (7Ah), TIMESTAMP1 (7Bh), TIMESTAMP2 (7Ch), and TIMESTAMP3 (7Dh)

R

Table 131. TIMESTAMP output registers

D31	D30	D29	D28	D27	D26	D25	D24
D23	D22	D21	D20	D19	D18	D17	D16
D15	D14	D13	D12	D11	D10	D9	D8
D7	D6	D5	D4	D3	D2	D1	D0

Table 132. TIMESTAMP output register description

D[31:0]	Timestamp output registers(1): 1LSB = 10 µs (typical)

1. *Timestamp information is not accurate in ultralow-power mode.*

9 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when the EMB_FUNC_REG_ACCESS bit is set to 1 in the FUNC_CFG_ACCESS (3Fh) register and the EMB_FUNC_EN bit is set to 1 in the CTRL4 (13h) register.

Table 133. Register address map - embedded functions

Name	Type	Register address		Default	Comment
		Hex	Binary		
PAGE_SEL	R/W	02	00000010	00000001	
RESERVED	-	03			
EMB_FUNC_EN_A	R/W	04	00000100	00000000	
EMB_FUNC_EN_B	R/W	05	00000101	00000000	
EMB_FUNC_EXEC_STATUS	R	07	00000111	output	
PAGE_ADDRESS	R/W	08	00001000	00000000	
PAGE_VALUE	R/W	09	00001001	00000000	
EMB_FUNC_INT	R/W	0A	00001010	00000000	
FSM_INT	R/W	0B	00001011	00000000	
RESERVED	-	0C			
MLC_INT	R/W	0D	00001101	00000000	
RESERVED	-	0E-11			
EMB_FUNC_STATUS	R	12	00010010	output	
FSM_STATUS	R	13	00010011	output	
RESERVED	-	14			
MLC_STATUS	R	15	00010101	output	
PAGE_RW	R/W	17	00010111	00000000	
EMB_FUNC_FIFO_EN	R/W	18	00011000		
RESERVED	-	19			
FSM_ENABLE	R/W	1A	00011010	00000000	
RESERVED	-	1B			
FSM_LONG_COUNTER_L	R/W	1C	00011100	00000000	
FSM_LONG_COUNTER_H	R/W	1D	00011101	00000000	
RESERVED	-	1E			
INT_ACK_MASK	R/W	1F	00011111	00000000	
FSM_OUTS1	R	20	00100000	output	
FSM_OUTS2	R	21	00100001	output	
FSM_OUTS3	R	22	00100010	output	
FSM_OUTS4	R	23	00100011	output	
FSM_OUTS5	R	24	00100100	output	
FSM_OUTS6	R	25	00100101	output	
FSM_OUTS7	R	26	00100110	output	
FSM_OUTS8	R	27	00100111	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
STEP_COUNTER_L	R	28	00101000	output	
STEP_COUNTER_H	R	29	00101001	output	
EMB_FUNC_SRC	R/W	2A	00101010	output	
RESERVED	-	2B			
EMB_FUNC_INIT_A	R/W	2C	00101100	00000000	
EMB_FUNC_INIT_B	R/W	2D	00101101	00000000	
RESERVED	-	2E-33			
MLC1_SRC	R	34	00110100	output	
MLC2_SRC	R	35	00110101	output	
MLC3_SRC	R	36	00110110	output	
MLC4_SRC	R	37	00110111	output	
FSM_ODR	R/W	39	00111001	01001000	
MLC_ODR	R/W	3A	00111010	00010001	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.
The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

10 Embedded functions register description

10.1 PAGE_SEL (02h)

Enable advanced features dedicated page (R/W)

Table 134. PAGE_SEL register

PAGE_SEL3	PAGE_SEL2	PAGE_SEL1	PAGE_SEL0	0(1)	0(1)	0(1)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 135. PAGE_SEL register description

PAGE_SEL[3:0]	Selects the advanced features dedicated page (from 0 to 3). Default value: 0000

10.2 EMB_FUNC_EN_A (04h)

Enable embedded functions register (R/W)

Table 136. EMB_FUNC_EN_A register

MLC_BEFORE_FSM_EN	0(1)	SIGN_MOTION_EN	TILT_EN	PEDO_EN	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 137. EMB_FUNC_EN_A register description

MLC_BEFORE_FSM_EN(1)	Enables machine learning core function. When the machine learning core is enabled by setting this bit to 1, the MLC algorithms are executed before the FSM programs. Default value: 0 (0: machine learning core function disabled; 1: machine learning core function enabled and executed before FSM programs)
SIGN_MOTION_EN	Enables significant motion detection function. Default value: 0 (0: significant motion detection function disabled; 1: significant motion detection function enabled)
TILT_EN	Enables tilt calculation. Default value: 0 (0: tilt algorithm disabled; 1: tilt algorithm enabled)
PEDO_EN	Enables pedometer algorithm. Default value: 0 (0: pedometer algorithm disabled; 1: pedometer algorithm enabled)

1. *The MLC_EN bit in the EMB_FUNC_EN_B (05h) register must be set to 0 when using this bit.*

10.3 EMB_FUNC_EN_B (05h)

Enable embedded functions register (R/W)

Table 138. EMB_FUNC_EN_B register

0(1)	0(1)	0(1)	MLC_EN	0(1)	0(1)	0(1)	FSM_EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 139. EMB_FUNC_EN_B register description

MLC_EN(1)	Enables machine learning core function. When the machine learning core is enabled by setting this bit to 1, the MLC algorithms are executed after executing the FSM programs. Default value: 0 (0: machine learning core function disabled; 1: machine learning core function enabled and executed after FSM programs)
FSM_EN	Enables finite state machine (FSM) function. Default value: 0 (0: FSM function disabled; 1: FSM function enabled)

1. *The MLC_BEFORE_FSM_EN bit in the EMB_FUNC_EN_A (04h) register must be set to 0 when using this bit.*

10.4 EMB_FUNC_EXEC_STATUS (07h)

Embedded functions execution status register (R)

Table 140. EMB_FUNC_EXEC_STATUS register

0	0	0	0	0	0	EMB_FUNC_EXEC_OVR	EMB_FUNC_ENDOP

Table 141. EMB_FUNC_EXEC_STATUS register description

EMB_FUNC_EXEC_OVR	This bit is set to 1 when the execution of the embedded functions program exceeds maximum time (new data are generated before the end of the algorithms). Default value: 0
EMB_FUNC_ENDOP	When this bit is set to 1, no embedded function is running. Default value: 0

10.5 PAGE_ADDRESS (08h)

Page address register (R/W)

Table 142. PAGE_ADDRESS register

PAGE_ADDR7	PAGE_ADDR6	PAGE_ADDR5	PAGE_ADDR4	PAGE_ADDR3	PAGE_ADDR2	PAGE_ADDR1	PAGE_ADDR0

Table 143. PAGE_ADDRESS register description

PAGE_ADDR[7:0]	After setting the bit PAGE_WRITE / PAGE_READ in register PAGE_RW (17h), this register is used to set the address of the register to be written/read in the advanced features page selected through the bits PAGE_SEL[3:0] in register PAGE_SEL (02h).

10.6 PAGE_VALUE (09h)

Page value register (R/W)

Table 144. PAGE_VALUE register

PAGE_ VALUE7	PAGE_ VALUE6	PAGE_ VALUE5	PAGE_ VALUE4	PAGE_ VALUE3	PAGE_ VALUE2	PAGE_ VALUE1	PAGE_ VALUE0

Table 145. PAGE_VALUE register description

PAGE_VALUE[7:0]	These bits are used to write (if the bit PAGE_WRITE = 1 in register PAGE_RW (17h)) or read (if the bit PAGE_READ = 1 in register PAGE_RW (17h)) the data at the address PAGE_ADDR[7:0] of the selected advanced features page.

10.7 EMB_FUNC_INT (0Ah)

INT pin control register (R/W)

Each bit in this register enables a signal to be carried over the INT pin. The pin's output supplies the OR combination of the selected signals.

Table 146. EMB_FUNC_INT register

INT_ FSM_LC	0(1)	INT_ SIG_MOT	INT_TILT	INT_STEP _DET	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 147. EMB_FUNC_INT register description

INT_FSM_LC(1)	Enables routing an FSM long counter timeout interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_SIG_MOT(1)	Enables routing a significant motion event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_TILT(1)	Enables routing a tilt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_STEP_DETECTOR(1)	Enables routing a pedometer step recognition event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)

1. *This bit is active if the INT_EMB_FUNC bit of MD1_CFG (1Fh) is set to 1.*

10.8 FSM_INT (0Bh)

INT pin control register (R/W)

Each bit in this register enables a signal to be carried over the INT pin. The pin's output supplies the OR combination of the selected signals.

Table 148. FSM_INT register

INT_FSM8	INT_FSM7	INT_FSM6	INT_FSM5	INT_FSM4	INT_FSM3	INT_FSM2	INT_FSM1

Table 149. FSM_INT register description

INT_FSM8(1)	Enables routing FSM8 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_FSM7(1)	Enables routing FSM7 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_FSM6(1)	Enables routing FSM6 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_FSM5(1)	Enables routing FSM5 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_FSM4(1)	Enables routing FSM4 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_FSM3(1)	Enables routing FSM3 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_FSM2(1)	Enables routing FSM2 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_FSM1(1)	Enables routing FSM1 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)

1. *This bit is active if the INT_EMB_FUNC bit of MD1_CFG (1Fh) is set to 1.*

10.9 MLC_INT (0Dh)

INT pin control register (R/W)

Each bit in this register enables a signal to be carried over the INT pin. The pin's output supplies the OR combination of the selected signals.

Table 150. MLC_INT register

0(1)	0(1)	0(1)	0(1)	INT_MLC4	INT_MLC3	INT_MLC2	INT_MLC1

1. *This bit must be set to 0 for the correct operation of the device.*

Table 151. MLC_INT register description

INT_MLC4(1)	Enables routing MLC4 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_MLC3(1)	Enables routing MLC3 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_MLC2(1)	Enables routing MLC2 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)
INT_MLC1(1)	Enables routing MLC1 interrupt event to the INT pin. Default value: 0 (0: routing to the INT pin disabled; 1: routing to the INT pin enabled)

1. *This bit is active if the INT_EMB_FUNC bit of MD1_CFG (1Fh) is set to 1.*

10.10 EMB_FUNC_STATUS (12h)

Embedded function status register (R)

Table 152. EMB_FUNC_STATUS register

IS_FSM_LC	0	IS_SIGMOT	IS_TILT	IS_STEP_DET	0	0	0

Table 153. EMB_FUNC_STATUS register description

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event (1: interrupt detected; 0: no interrupt)
IS_SIGMOT	Interrupt status bit for significant motion detection (1: interrupt detected; 0: no interrupt)
IS_TILT	Interrupt status bit for tilt detection (1: interrupt detected; 0: no interrupt)
IS_STEP_DET	Interrupt status bit for step detection (1: interrupt detected; 0: no interrupt)

10.11 FSM_STATUS (13h)

Finite state machine status register (R)

Table 154. FSM_STATUS register

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1

Table 155. FSM_STATUS register description

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

10.12 MLC_STATUS (15h)

Machine learning core status register (R)

Table 156. MLC_STATUS register

0	0	0	0	IS_MLC4	IS_MLC3	IS_MLC	IS_MLC1

Table 157. MLC_STATUS register description

IS_MLC4	Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC3	Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC2	Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC1	Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt)

10.13 PAGE_RW (17h)

Enable read and write mode of advanced features dedicated page (R/W)

Table 158. PAGE_RW register

EMB_ FUNC_LIR	PAGE_ WRITE	PAGE_ READ	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 159. PAGE_RW register description

EMB_FUNC_LIR	Latched interrupt mode for embedded functions. Default value: 0 (0: embedded functions interrupt request not latched; 1: embedded functions interrupt request latched)
PAGE_WRITE	Enable writes to the selected advanced features dedicated page.(1) Default value: 0 (1: enable; 0: disable)
PAGE_READ	Enable reads from the selected advanced features dedicated page.(1) Default value: 0 (1: enable; 0: disable)

1. *Page selected by PAGE_SEL[3:0] in PAGE_SEL (02h) register.*

10.14 EMB_FUNC_FIFO_EN (18h)

Embedded functions FIFO configuration register (R/W)

Table 160. EMB_FUNC_FIFO_EN register

0(1)	0(1)	0(1)	0(1)	FSM_FIFO_EN	MLC_FILTER_ FEATURE_FIFO _EN	MLC_ FIFO_EN	STEP_COUNTER _FIFO_EN

1. *This bit must be set to 0 for the correct operation of the device.*

Table 161. EMB_FUNC_FIFO_EN register description

FSM_FIFO_EN(1)	Enables batching finite state machine results in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
MLC_FILTER_FEATURE_FIFO_EN(1)	Enables batching machine learning core filters and features in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
MLC_FIFO_EN(1)	Enables batching machine learning core results in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)
STEP_COUNTER_FIFO_EN(1)	Enables batching step counter values in the FIFO buffer. Default value: 0 (0: disabled; 1: enabled)

1. *When this bit is set to 1, the FIFO must be enabled in continuous mode.*

10.15 FSM_ENABLE (1Ah)

Enable FSM register (R/W)

Table 162. FSM_ENABLE register

FSM8_EN	FSM7_EN	FSM6_EN	FSM5_EN	FSM4_EN	FSM3_EN	FSM2_EN	FSM1_EN

Table 163. FSM_ENABLE register description

FSM8_EN	Enables FSM8. Default value: 0 (0: FSM8 disabled; 1: FSM8 enabled)
FSM7_EN	Enables FSM7. Default value: 0 (0: FSM7 disabled; 1: FSM7 enabled)
FSM6_EN	Enables FSM6. Default value: 0 (0: FSM6 disabled; 1: FSM6 enabled)
FSM5_EN	Enables FSM5. Default value: 0 (0: FSM5 disabled; 1: FSM5 enabled)
FSM4_EN	Enables FSM4. Default value: 0 (0: FSM4 disabled; 1: FSM4 enabled)
FSM3_EN	Enables FSM3. Default value: 0 (0: FSM3 disabled; 1: FSM3 enabled)
FSM2_EN	Enables FSM2. Default value: 0 (0: FSM2 disabled; 1: FSM2 enabled)
FSM1_EN	Enables FSM1. Default value: 0 (0: FSM1 disabled; 1: FSM1 enabled)

10.16 FSM_LONG_COUNTER_L (1Ch) and FSM_LONG_COUNTER_H (1Dh)

FSM long counter status register (R/W)

Long counter value is an unsigned integer value (16-bit format).

Table 164. FSM_LONG_COUNTER_L register

FSM_LC_7	FSM_LC_6	FSM_LC_5	FSM_LC_4	FSM_LC_3	FSM_LC_2	FSM_LC_1	FSM_LC_0

Table 165. FSM_LONG_COUNTER_L register description

FSM_LC_[7:0]	Long counter current value (LSbyte). Default value: 00000000

Table 166. FSM_LONG_COUNTER_H register

-	FSM_LC_14	FSM_LC_13	FSM_LC_12	FSM_LC_11	FSM_LC_10	FSM_LC_9	FSM_LC_8

Table 167. FSM_LONG_COUNTER_H register description

FSM_LC_[14:8]	Long counter current value (MSbyte). Default value: 00000000

10.17 INT_ACK_MASK (1Fh)

Reset status register (R/W)

Table 168. INT_ACK_MASK register

IACK_ MASK7	IACK_ MASK6	IACK_ MASK5	IACK_ MASK4	IACK_ MASK3	IACK_ MASK2	IACK_ MASK1	IACK_ MASK0

Table 169. INT_ACK_MASK register description

IACK_MASK7	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (34h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (35h) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (36h) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 7 of the status register is not reset. When this bit is set to 0, bit 7 of the status register is reset. Default value: 0
IACK_MASK6	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (34h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (35h) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (36h) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 6 of the status register is not reset. When this bit is set to 0, bit 6 of the status register is reset. Default value: 0
IACK_MASK5	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (34h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (35h) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (36h) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 5 of the status register is not reset. When this bit is set to 0, bit 5 of the status register is reset. Default value: 0
IACK_MASK4	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (34h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (35h) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (36h) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 4 of the status register is not reset. When this bit is set to 0, bit 4 of the status register is reset. Default value: 0
IACK_MASK3	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (34h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (35h) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (36h) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 3 of the status register is not reset. When this bit is set to 0, bit 3 of the status register is reset. Default value: 0
IACK_MASK2	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (34h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (35h) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (36h) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 2 of the status register is not reset. When this bit is set to 0, bit 2 of the status register is reset. Default value: 0
IACK_MASK1	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (34h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (35h) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (36h) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 1 of the status register is not reset. When this bit is set to 0, bit 1 of the status register is reset. Default value: 0
IACK_MASK0	If set to 1, when reading the EMB_FUNC_STATUS (12h) / EMB_FUNC_STATUS_MAINPAGE (34h), FSM_STATUS (13h) / FSM_STATUS_MAINPAGE (35h) and MLC_STATUS (15h) / MLC_STATUS_MAINPAGE (36h) registers in latched mode (when the EMB_FUNC_LIR bit is set to 1 in the PAGE_RW (17h) register), bit 0 of the status register is not reset. When this bit is set to 0, bit 0 of the status register is reset. Default value: 0

10.18 FSM_OUTS1 (20h)

FSM1 output register (R)

Table 170. FSM_OUTS1 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 171. FSM_OUTS1 register description

P_X	FSM1 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM1 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM1 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM1 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM1 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM1 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM1 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM1 output: negative event detected on the vector. (0: event not detected; 1: event detected)

10.19 FSM_OUTS2 (21h)

FSM2 output register (R)

Table 172. FSM_OUTS2 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 173. FSM_OUTS2 register description

P_X	FSM2 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM2 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM2 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM2 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM2 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM2 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM2 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM2 output: negative event detected on the vector. (0: event not detected; 1: event detected)

10.20 FSM_OUTS3 (22h)

FSM3 output register (R)

Table 174. FSM_OUTS3 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 175. FSM_OUTS3 register description

P_X	FSM3 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM3 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM3 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM3 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM3 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM3 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM3 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM3 output: negative event detected on the vector. (0: event not detected; 1: event detected)

10.21 FSM_OUTS4 (23h)

FSM4 output register (R)

Table 176. FSM_OUTS4 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 177. FSM_OUTS4 register description

P_X	FSM4 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM4 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM4 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM4 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM4 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM4 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM4 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM4 output: negative event detected on the vector. (0: event not detected; 1: event detected)

10.22 FSM_OUTS5 (24h)

FSM5 output register (R)

Table 178. FSM_OUTS5 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 179. FSM_OUTS5 register description

P_X	FSM5 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM5 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM5 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM5 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM5 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM5 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM5 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM5 output: negative event detected on the vector. (0: event not detected; 1: event detected)

10.23 FSM_OUTS6 (25h)

FSM6 output register (R)

Table 180. FSM_OUTS6 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 181. FSM_OUTS6 register description

P_X	FSM6 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM6 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM6 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM6 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM6 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM6 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM6 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM6 output: negative event detected on the vector. (0: event not detected; 1: event detected)

10.24 FSM_OUTS7 (26h)

FSM7 output register (R)

Table 182. FSM_OUTS7 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 183. FSM_OUTS7 register description

P_X	FSM7 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM7 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM7 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM7 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM7 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM7 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM7 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM7 output: negative event detected on the vector. (0: event not detected; 1: event detected)

10.25 FSM_OUTS8 (27h)

FSM8 output register (R)

Table 184. FSM_OUTS8 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 185. FSM_OUTS8 register description

P_X	FSM8 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM8 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM8 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM8 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM8 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM8 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM8 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM8 output: negative event detected on the vector. (0: event not detected; 1: event detected)

10.26 STEP_COUNTER_L (28h) and STEP_COUNTER_H (29h)

Step counter output register (R)

Table 186. STEP_COUNTER_L register

STEP_7	STEP_6	STEP_5	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0

Table 187. STEP_COUNTER_L register description

STEP_[7:0]	Step counter output (LSbyte)

Table 188. STEP_COUNTER_H register

STEP_15	STEP_14	STEP_13	STEP_12	STEP_11	STEP_10	STEP_9	STEP_8

Table 189. STEP_COUNTER_H register description

STEP_[15:8]	Step counter output (MSbyte)

10.27 EMB_FUNC_SRC (2Ah)

Embedded function source register (R/W)

Table 190. EMB_FUNC_SRC register

PEDO_ RST_STEP	0(1)	STEP_ DETECTED	STEP_COUNT _DELTA_IA	STEP_ OVERFLOW	STEPCOUNTER _BIT_SET	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 191. EMB_FUNC_SRC register description

PEDO_RST_STEP	Reset pedometer step counter. Read/write bit. (0: disabled; 1: enabled)
STEP_DETECTED	Step detector event detection status. Read-only bit. (0: step detection event not detected; 1: step detection event detected)
STEP_COUNT_DELTA_IA	Pedometer step recognition on delta time status. Read-only bit. (0: no step recognized during delta time; 1: at least one step recognized during delta time)
STEP_OVERFLOW	Step counter overflow status. Read-only bit. (0: step counter value < 2^{16}; 1: step counter value reached 2^{16})
STEPCOUNTER_BIT_SET	This bit is equal to 1 when the step count is increased. If a timer period is programmed in PEDO_SC_DELTAT_L (AAh) and PEDO_SC_DELTAT_H (ABh) embedded advanced features (page 1) registers, this bit is kept to 0. Read-only bit.

10.28 EMB_FUNC_INIT_A (2Ch)

Embedded functions initialization register (R/W)

Table 192. EMB_FUNC_INIT_A register

MLC_BEFORE_FSM_INIT	0(1)	SIG_MOT_INIT	TILT_INIT	STEP_DET_INIT	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 193. EMB_FUNC_INIT_A register description

MLC_BEFORE_FSM_INIT	Machine learning core initialization request (MLC executed before FSM). Default value: 0
SIG_MOT_INIT	Significant motion detection algorithm initialization request. Default value: 0
TILT_INIT	Tilt algorithm initialization request. Default value: 0
STEP_DET_INIT	Pedometer step counter/detector algorithm initialization request. Default value: 0

10.29 EMB_FUNC_INIT_B (2Dh)

Embedded functions initialization register (R/W)

Table 194. EMB_FUNC_INIT_B register

0(1)	0(1)	0(1)	MLC_INIT	0(1)	0(1)	0(1)	FSM_INIT

1. *This bit must be set to 0 for the correct operation of the device.*

Table 195. EMB_FUNC_INIT_B register description

MLC_INIT	Machine learning core initialization request (MLC executed after FSM). Default value: 0
FSM_INIT	FSM initialization request. Default value: 0

10.30 MLC1_SRC (34h)

Machine learning core source register (R)

Table 196. MLC1_SRC register

MLC1_SRC_7	MLC1_SRC_6	MLC1_SRC_5	MLC1_SRC_4	MLC1_SRC_3	MLC1_SRC_2	MLC1_SRC_1	MLC1_SRC_0

Table 197. MLC1_SRC register description

MLC1_SRC_[7:0]	Output value of MLC1 decision tree

10.31 MLC2_SRC (35h)

Machine learning core source register (R)

Table 198. MLC2_SRC register

MLC2_ SRC_7	MLC2_ SRC_6	MLC2_ SRC_5	MLC2_ SRC_4	MLC2_ SRC_3	MLCS2_ SRC_2	MLC2_ SRC_1	MLC2_ SRC_0

Table 199. MLC2_SRC register description

MLC2_SRC_[7:0]	Output value of MLC2 decision tree

10.32 MLC3_SRC (36h)

Machine learning core source register (R)

Table 200. MLC3_SRC register

MLC3_ SRC_7	MLC3_ SRC_6	MLC3_ SRC_5	MLC3_ SRC_4	MLC3_ SRC_3	MLC3_ SRC_2	MLC3_ SRC_1	MLC3_ SRC_0

Table 201. MLC3_SRC register description

MLC3_SRC_[7:0]	Output value of MLC3 decision tree

10.33 MLC4_SRC (37h)

Machine learning core source register (R)

Table 202. MLC4_SRC register

MLC4_ SRC_7	MLC4_ SRC_6	MLC4_ SRC_5	MLC4_ SRC_4	MLC4_ SRC_3	MLC4_ SRC_2	MLC4_ SRC_1	MLC4_ SRC_0

Table 203. MLC4_SRC register description

MLC4_SRC_[7:0]	Output value of MLC4 decision tree

10.34 FSM_ODR (39h)

Finite state machine output data rate configuration register (R/W)

Table 204. FSM_ODR register

0(1)	1(2)	FSM_ODR_2	FSM_ODR_1	FSM_ODR_0	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 205. FSM_ODR register description

FSM_ODR_[2:0]	If the device is not set in the AH / vAFE only state, the finite state machine ODR configuration is: (000: 12.5 Hz; 001: 25 Hz (default); 010: 50 Hz; 011: 100 Hz; 100: 200 Hz; 101: 400 Hz; 110: 800 Hz) If the device is set in the AH / vAFE only state (see Section 2.6: Analog hub / vAFE only state), the finite state machine ODR configuration is: (000: 50 Hz; 001: 100 Hz (default); 010: 200 Hz; 011: 400 Hz; 100: 800 Hz; 101: 1600 Hz (available if the HP_EN bit is set to 0 in the CTRL3 (12h) register); 110: reserved)

10.35 MLC_ODR (3Ah)

Machine learning core output data rate configuration register (R/W)

Table 206. MLC_ODR register

0(1)	MLC_ODR_2	MLC_ODR_1	MLC_ODR_0	0(1)	0(1)	0(1)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 207. MLC_ODR register description

MLC_ODR_[2:0]	If the device is not set in the AH / vAFE only state, the machine learning core ODR configuration is: (000: 12.5 Hz; 001: 25 Hz (default); 010: 50 Hz; 011: 100 Hz; 100: 200 Hz) If the device is set in the AH / vAFE only state (see Section 2.6: Analog hub / vAFE only state), the machine learning core ODR configuration is: (000: 50 Hz; 001: 100 Hz (default); 010: 200 Hz; 011: 400 Hz; 100: 800 Hz; 101: 1600 Hz (available if the HP_EN bit is set to 0 in the CTRL3 (12h) register); 110: reserved)

11 Embedded advanced features pages

The table given below provides a list of the registers for the embedded advanced features page 0. These registers are accessible when PAGE_SEL[3:0] are set to 0000 in PAGE_SEL (02h).

Note: The content of these registers is loaded when the embedded functions are enabled by setting the EMB_FUNC_EN bit to 1 in the CTRL4 (13h) register. The embedded functions must be enabled in order for these registers to become accessible.

Table 208. Register address map - embedded advanced features page 0

Name	Type	Register address		Default	Comment
		Hex	Binary		
FSM_LC_TIMEOUT_L	R/W	54	01010100	00000000	
FSM_LC_TIMEOUT_H	R/W	55	01010101	00000000	
FSM_PROGRAMS	R/W	56	01010110	00000000	
FSM_START_ADD_L	R/W	58	01011000	00000000	
FSM_START_ADD_H	R/W	59	01011001	00000000	
PEDO_CMD_REG	R/W	5D	01011101	00000000	
PEDO_DEB_STEPS_CONF	R/W	5E	01011110	00001010	
PEDO_SC_DELTAT_L	R/W	AA	10101010	00000000	
PEDO_SC_DELTAT_H	R/W	AB	10101011	00000000	
AH_BIO_SENSITIVITY_L	R/W	B6	10110110	01100110	
AH_BIO_SENSITIVITY_H	R/W	B7	10110111	00010010	
SMART_POWER_CTRL	R/W	D2	11010010	10000000	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

Write procedure example: write value 06h in register at address 5Eh (PEDO_DEB_STEPS_CONF) in Page 0

1. Write bit EMB_FUNC_REG_ACCESS = 1 in FUNC_CFG_ACCESS (3Fh) // Enable access to embedded functions registers
2. Write bit PAGE_WRITE = 1 in PAGE_RW (17h) register // Select write operation mode
3. Write 0000 in PAGE_SEL[3:0] field of register PAGE_SEL (02h) // Select page 0
4. Write 5Eh in PAGE_ADDRESS (08h) register // Set address
5. Write 06h in PAGE_VALUE (09h) register // Set value to be written
6. Write bit PAGE_WRITE = 0 in PAGE_RW (17h) register // Write operation disabled
7. Write bit EMB_FUNC_REG_ACCESS = 0 in FUNC_CFG_ACCESS (3Fh) // Disable access to embedded functions registers

Read procedure example: read value of register at address 5Eh (PEDO_DEB_STEPS_CONF) in Page 0

1.	Write bit EMB_FUNC_REG_ACCESS = 1 in FUNC_CFG_ACCESS (3Fh)	// Enable access to embedded functions registers
2.	Write bit PAGE_READ = 1 in PAGE_RW (17h) register	// Select read operation mode
3.	Write 0000 in PAGE_SEL[3:0] field of register PAGE_SEL (02h)	// Select page 0
4.	Write 5Eh in PAGE_ADDRESS (08h) register	// Set address
5.	Read value of PAGE_VALUE (09h) register	// Get register value
6.	Write bit PAGE_READ = 0 in PAGE_RW (17h) register	// Read operation disabled
7.	Write bit EMB_FUNC_REG_ACCESS = 0 in FUNC_CFG_ACCESS (3Fh)	// Disable access to embedded functions registers

Note: Steps 1 and 2 of both procedures are intended to be performed at the beginning of the procedure. Steps 6 and 7 of both procedures are intended to be performed at the end of the procedure. If the procedure involves multiple operations, only steps 3, 4 and 5 must be repeated for each operation. If, in particular, the multiple operations involve consecutive registers, only step 5 can be performed.

12 Embedded advanced features register description

12.1 Page 0 - embedded advanced features registers

12.1.1 FSM_LC_TIMEOUT_L (54h) and FSM_LC_TIMEOUT_H (55h)

FSM long counter timeout register (R/W)

The long counter timeout value is an unsigned integer value (16-bit format). When the long counter value reached this value, the FSM generates an interrupt.

Table 209. FSM_LC_TIMEOUT_L register

FSM_LC_TIMEOUT7	FSM_LC_TIMEOUT6	FSM_LC_TIMEOUT5	FSM_LC_TIMEOUT4	FSM_LC_TIMEOUT3	FSM_LC_TIMEOUT2	FSM_LC_TIMEOUT1	FSM_LC_TIMEOUT0

Table 210. FSM_LC_TIMEOUT_L register description

FSM_LC_TIMEOUT[7:0]	FSM long counter timeout value (LSbyte). Default value: 00000000

Table 211. FSM_LC_TIMEOUT_H register

FSM_LC_TIMEOUT15	FSM_LC_TIMEOUT14	FSM_LC_TIMEOUT13	FSM_LC_TIMEOUT12	FSM_LC_TIMEOUT11	FSM_LC_TIMEOUT10	FSM_LC_TIMEOUT9	FSM_LC_TIMEOUT8

Table 212. FSM_LC_TIMEOUT_H register description

FSM_LC_TIMEOUT[15:8]	FSM long counter timeout value (MSbyte). Default value: 00000000

12.1.2 FSM_PROGRAMS (56h)

FSM number of programs register (R/W)

Table 213. FSM_PROGRAMS register

FSM_N_PROG7	FSM_N_PROG6	FSM_N_PROG5	FSM_N_PROG4	FSM_N_PROG3	FSM_N_PROG2	FSM_N_PROG1	FSM_N_PROG0

Table 214. FSM_PROGRAMS register description

FSM_N_PROG[7:0]	Number of FSM programs; must be less than or equal to 8. Default value: 00000000

12.1.3 FSM_START_ADD_L (58h) and FSM_START_ADD_H (59h)

FSM start address register (R/W). First available address is 0x19C.

Table 215. FSM_START_ADD_L register

FSM_START7	FSM_START6	FSM_START5	FSM_START4	FSM_START3	FSM_START2	FSM_START1	FSM_START0

Table 216. FSM_START_ADD_L register description

FSM_START[7:0]	FSM start address value (LSbyte). Default value: 00000000

Table 217. FSM_START_ADD_H register

FSM_START15	FSM_START14	FSM_START13	FSM_START12	FSM_START11	FSM_START10	FSM_START9	FSM_START8

Table 218. FSM_START_ADD_H register description

FSM_START[15:8]	FSM start address value (MSbyte). Default value: 00000000

12.1.4 PEDO_CMD_REG (5Dh)

Pedometer configuration register (R/W)

Table 219. PEDO_CMD_REG register

0(1)	0(1)	0(1)	0(1)	CARRY_COUNT_EN	FP_REJECTION_EN	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 220. PEDO_CMD_REG register description

CARRY_COUNT_EN	Set when user wants to generate interrupt only on count overflow event.
FP_REJECTION_EN(1)	Enables the false-positive rejection feature

1. *This bit is active if the MLC_EN bit of EMB_FUNC_EN_B (05h) or the MLC_BEFORE_FSM_EN bit in the EMB_FUNC_EN_A (04h) register is set to 1.*

12.1.5 PEDO_DEB_STEPS_CONF (5Eh)

Pedometer debounce configuration register (R/W)

Table 221. PEDO_DEB_STEPS_CONF register

DEB_ STEP7	DEB_ STEP6	DEB_ STEP5	DEB_ STEP4	DEB_ STEP3	DEB_ STEP2	DEB_ STEP1	DEB_ STEP0

Table 222. PEDO_DEB_STEPS_CONF register description

DEB_STEP[7:0]	Debounce threshold. Minimum number of steps to increment the step counter (debounce). Default value: 00001010

12.1.6 PEDO_SC_DELTAT_L (AAh) and PEDO_SC_DELTAT_H (ABh)

Time period register for step detection on delta time (R/W)

Table 223. PEDO_SC_DELTAT_L register

PD_SC_7	PD_SC_6	PD_SC_5	PD_SC_4	PD_SC_3	PD_SC_2	PD_SC_1	PD_SC_0

Table 224. PEDO_SC_DELTAT_H register

PD_SC_15	PD_SC_14	PD_SC_13	PD_SC_12	PD_SC_11	PD_SC_10	PD_SC_9	PD_SC_8

Table 225. PEDO_SC_DELTAT_H/L register description

PD_SC_[15:0]	Time period value (1LSB = 2.56 ms)

12.1.7 AH_BIO_SENSITIVITY_L (B6h) and AH_BIO_SENSITIVITY_H (B7h)

Analog hub / vAFE sensor sensitivity value register (R/W)

This sensitivity value is also applied to the data processed in the finite state machine (FSM) and machine learning core (MLC) blocks.

This register corresponds to the conversion value of the analog hub / vAFE sensor. The register value is expressed as half-precision floating-point format: SEEEEEFFFFFFFFFF (S: 1 sign bit; E: 5 exponent bits; F: 10 fraction bits).

The default value of AH_BIO_S_[15:0] is 0x1266; when the analog hub / vAFE is enabled, the user needs to modify the sensitivity accordingly.

Table 226. AH_BIO_SENSITIVITY_L register

AH_BIO_S_7	AH_BIO_S_6	AH_BIO_S_5	AH_BIO_S_4	AH_BIO_S_3	AH_BIO_S_2	AH_BIO_S_1	AH_BIO_S_0

Table 227. AH_BIO_SENSITIVITY_L register description

AH_BIO_S_[7:0]	Analog hub / vAFE sensitivity (LSbyte). Default value: 01100110

Table 228. AH_BIO_SENSITIVITY_H register

AH_BIO_S_15	AH_BIO_S_14	AH_BIO_S_13	AH_BIO_S_12	AH_BIO_S_11	AH_BIO_S_10	AH_BIO_S_9	AH_BIO_S_8

Table 229. AH_BIO_SENSITIVITY_H register description

AH_BIO_S_[15:8]	Analog hub / vAFE sensitivity (MSbyte). Default value: 00010010

12.1.8 SMART_POWER_CTRL (D2h)

Smart power management configuration register (R/W)

Table 230. SMART_POWER_CTRL register

SMART_POWER_CTRL_DUR3	SMART_POWER_CTRL_DUR2	SMART_POWER_CTRL_DUR1	SMART_POWER_CTRL_DUR0	SMART_POWER_CTRL_WIN3	SMART_POWER_CTRL_WIN2	SMART_POWER_CTRL_WIN1	SMART_POWER_CTRL_WIN0

Table 231. SMART_POWER_CTRL register description

SMART_POWER_CTRL_DUR[3:0]	Sets the value of the duration threshold for the smart power management feature. The actual value is the value of the ODR period multiplied by SMART_POWER_CTRL_DUR[3:0] / 16.
SMART_POWER_CTRL_WIN[3:0]	Sets the number of consecutive windows during which the smart power management feature is evaluated. The actual number is SMART_POWER_CTRL_WIN[3:0] * 16.

13 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

13.1 Soldering information

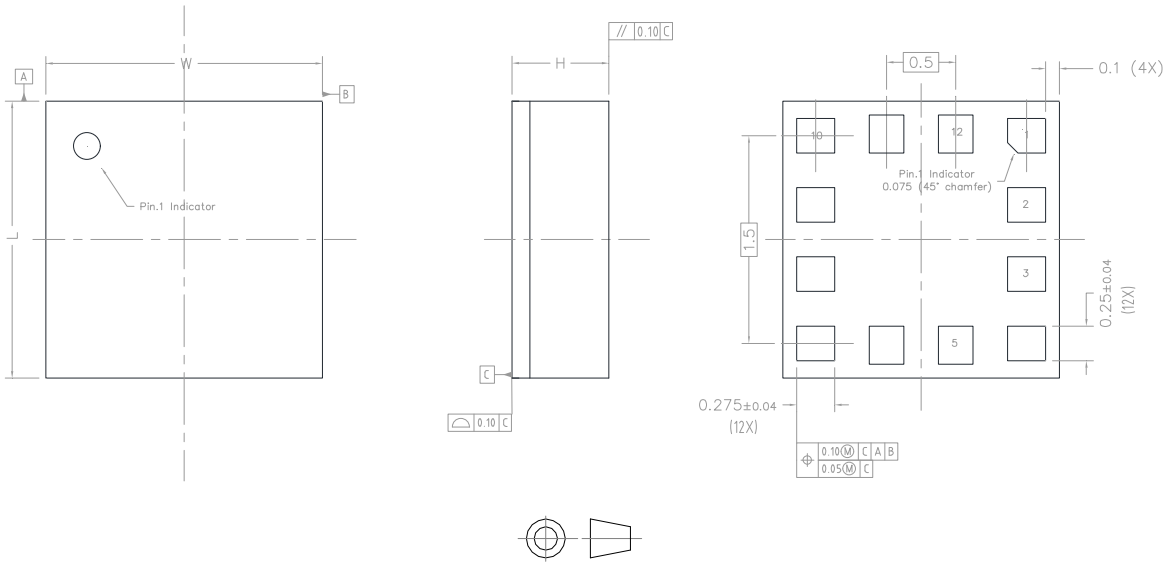
The LGA package is compliant with the ECOPACK and RoHS standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

For the land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

13.2 LGA-12L package information

Figure 18. LGA-12L 2.0 x 2.0 x 0.74 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified.
General Tolerance is +/-0.1mm unless otherwise specified.

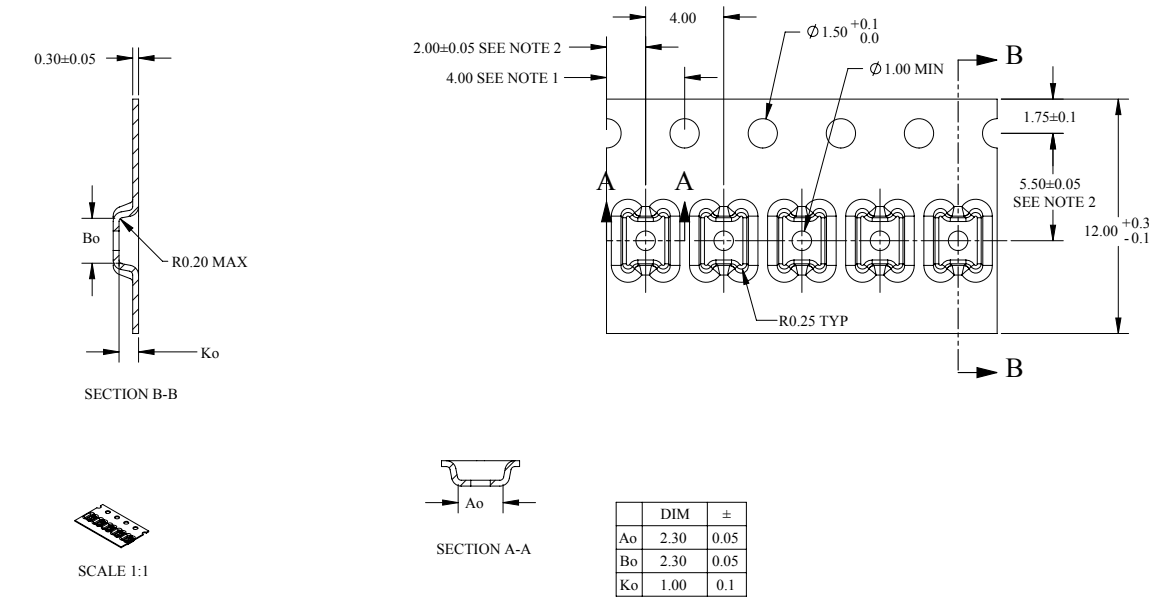
OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2	±0.1
Width [W]	2	±0.1
Height [H]	0.74 MAX	/

DM00794797_1

13.3 LGA-12L packing information

Figure 19. Carrier tape information for LGA-12L package



	DIM	±
Ao	2.30	0.05
Bo	2.30	0.05
Ko	1.00	0.1

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 20. LGA-12L package orientation in carrier tape

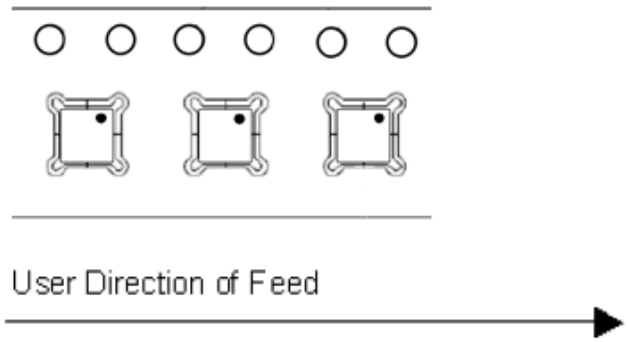


Figure 21. **Reel information for carrier tape of LGA-12L package**

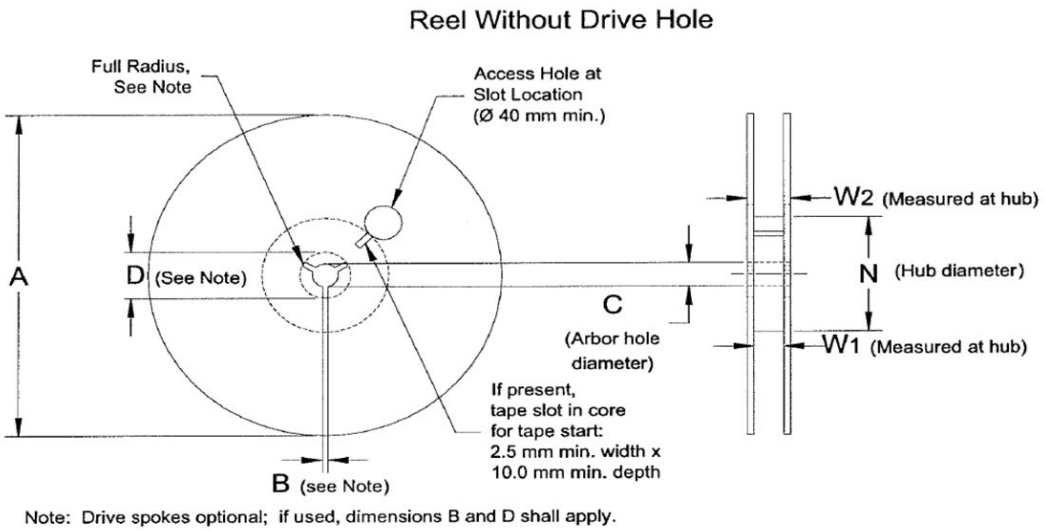


Table 232. **Reel dimensions for carrier tape of LGA-12L package**

Reel dimensions (mm)	
A (max)	609
B (min)	1.5
C	13.0 +0.5/-0.2
D (min)	20.2
N	177 ±2
W (tape width)	12
W1	12.4 +2/-0
W2 (max)	18.4

Revision history

Table 233. **Document revision history**

Date	Version	Changes
13-Aug-2024	1	Initial release
24-Oct-2024	2	Updated product resources on page 1 Updated Table 8. Absolute maximum ratings Updated pin status for pin 12 in Table 17. Internal pin status Updated Table 107. Identification of sensor in FIFO Updated first available address in FSM_START_ADD_L (58h) and FSM_START_ADD_H (59h) Updated Table 225. PEDO_SC_DELTAT_H/L register description Updated default values in AH_BIO_SENSITIVITY_L (B6h) and AH_BIO_SENSITIVITY_H (B7h)
22-Nov-2024	3	Updated supply current (high-performance mode, ultralow-power mode, and power-down mode) in Table 4. Electrical characteristics
25-Mar-2025	4	Updated Product resources and Section 2.3: vAFE description
28-May-2025	5	Added Section 13.3: LGA-12L packing information
04-Jun-2025	6	Removed footnote from bit7 in Table 103. FUNC_CFG_ACCESS register
22-May-2026	7	Updated Section 2.3: vAFE description Updated Section 6.1: FIFO Updated EMB_FUNC_EN bit in CTRL4 (13h) register

Contents

1 **Block diagram and pin description** 3
1.1 Block diagram 3
1.2 Pin description 4
2 **Functionality** 5
2.1 Operating modes 5
2.2 Biosensor functionality 5
2.3 vAFE description 5
2.4 One-shot mode 5
2.5 Power-up sequence and active mode configuration 6
2.5.1 Power-up command 6
2.6 Analog hub / vAFE only state 6
2.7 Activity/inactivity, Android stationary/motion detection functions 7
2.8 Interrupt event recognition 8
3 **Electrical and mechanical specifications** 9
3.1 Electrical characteristics 9
3.2 Mechanical characteristics 11
3.3 Communication interface characteristics 12
3.3.1 SPI - serial peripheral interface 12
3.3.2 I²C - inter-IC control interface 14
3.4 Absolute maximum ratings 15
3.5 Terminology 16
3.5.1 Accelerometer sensitivity 16
3.5.2 Accelerometer zero-*g* level offset 16
4 **Digital interfaces** 17
4.1 I²C serial interface 17
4.1.1 I²C operation 18
4.2 SPI bus interface 19
4.2.1 SPI read 20
4.2.2 SPI write 21
4.2.3 SPI read in 3-wire mode 21
4.3 MIPI I3C® interface 22
4.3.1 MIPI I3C® target interface 22
4.3.2 MIPI I3C® CCC supported commands 23
4.3.3 Antispike filter management on mixed I²C/MIPI I3C® bus 24

5 Application hints 25
6 Digital main blocks and embedded low-power features 27
6.1 FIFO 27
6.1.1 Bypass mode 28
6.1.2 FIFO mode 28
6.1.3 Continuous mode 28
6.1.4 Continuous-to-FIFO mode 28
6.1.5 Bypass-to-continuous mode 29
6.1.6 Bypass-to-FIFO 29
6.1.7 FIFO reading procedure 29
6.1.8 FIFO empty condition 29
6.2 Pedometer functions: step detector and step counters 30
6.3 Pedometer algorithm 30
6.4 Tilt detection 31
6.5 Significant motion detection 31
6.6 Finite state machine 31
6.7 Machine learning core 32
6.8 Adaptive self-configuration (ASC) 33
7 Register mapping 34
8 Register description 36
8.1 EXT_CLK_CFG (08h) 36
8.2 PIN_CTRL (0Ch) 36
8.3 WAKE_UP_DUR_EXT (0Eh) 37
8.4 WHO_AM_I (0Fh) 37
8.5 CTRL1 (10h) 37
8.6 CTRL2 (11h) 38
8.7 CTRL3 (12h) 38
8.8 CTRL4 (13h) 39
8.9 CTRL5 (14h) 40
8.10 FIFO_CTRL (15h) 42
8.11 FIFO_WTM (16h) 43
8.12 INTERRUPT_CFG (17h) 43
8.13 SIXD (18h) 44
8.14 WAKE_UP_THS (1Ch) 44
8.15 WAKE_UP_DUR (1Dh) 45
8.16 FREE_FALL (1Eh) 45

8.17 MD1_CFG (1Fh) . . . 46
8.18 WAKE_UP_SRC (21h) . . . 47
8.19 TAP_SRC (22h) . . . 48
8.20 SIXD_SRC (23h) . . . 48
8.21 ALL_INT_SRC (24h) . . . 49
8.22 STATUS (25h) . . . 49
8.23 FIFO_STATUS1 (26h) . . . 50
8.24 FIFO_STATUS2 (27h) . . . 50
8.25 OUT_X_L (28h) . . . 50
8.26 OUT_X_H (29h) . . . 50
8.27 OUT_Y_L (2Ah) . . . 51
8.28 OUT_Y_H (2Bh) . . . 51
8.29 OUT_Z_L (2Ch) . . . 51
8.30 OUT_Z_H (2Dh) . . . 51
8.31 OUT_AH_BIO_L (2Eh) . . . 52
8.32 OUT_AH_BIO_H (2Fh) . . . 52
8.33 AH_BIO_CFG1 (30h) . . . 52
8.34 AH_BIO_CFG2 (31h) . . . 53
8.35 AH_BIO_CFG3 (32h) . . . 54
8.36 I3C_IF_CTRL (33h) . . . 54
8.37 EMB_FUNC_STATUS_MAINPAGE (34h) . . . 54
8.38 FSM_STATUS_MAINPAGE (35h) . . . 55
8.39 MLC_STATUS_MAINPAGE (36h) . . . 55
8.40 EN_DEVICE_CONFIG (3Eh) . . . 55
8.41 FUNC_CFG_ACCESS (3Fh) . . . 56
8.42 FIFO_DATA_OUT_TAG (40h) . . . 56
8.43 FIFO_DATA_OUT_X_L (41h) and FIFO_DATA_OUT_X_H (42h) . . . 57
8.44 FIFO_DATA_OUT_Y_L (43h) and FIFO_DATA_OUT_Y_H (44h) . . . 57
8.45 FIFO_DATA_OUT_Z_L (45h) and FIFO_DATA_OUT_Z_H (46h) . . . 57
8.46 FIFO_BATCH_DEC (47h) . . . 58
8.47 TAP_CFG0 (6Fh) . . . 59
8.48 TAP_CFG1 (70h) . . . 59
8.49 TAP_CFG2 (71h) . . . 60
8.50 TAP_CFG3 (72h) . . . 60
8.51 TAP_CFG4 (73h) . . . 60
8.52 TAP_CFG5 (74h) . . . 61

8.53 TAP_CFG6 (75h) . . . 61
8.54 TIMESTAMP0 (7Ah), TIMESTAMP1 (7Bh), TIMESTAMP2 (7Ch), and TIMESTAMP3 (7Dh) . . . 62
9 Embedded functions register mapping . . . 63
10 Embedded functions register description . . . 65
10.1 PAGE_SEL (02h) . . . 65
10.2 EMB_FUNC_EN_A (04h) . . . 65
10.3 EMB_FUNC_EN_B (05h) . . . 66
10.4 EMB_FUNC_EXEC_STATUS (07h) . . . 66
10.5 PAGE_ADDRESS (08h) . . . 66
10.6 PAGE_VALUE (09h) . . . 67
10.7 EMB_FUNC_INT (0Ah) . . . 67
10.8 FSM_INT (0Bh) . . . 68
10.9 MLC_INT (0Dh) . . . 69
10.10 EMB_FUNC_STATUS (12h) . . . 69
10.11 FSM_STATUS (13h) . . . 70
10.12 MLC_STATUS (15h) . . . 70
10.13 PAGE_RW (17h) . . . 71
10.14 EMB_FUNC_FIFO_EN (18h) . . . 71
10.15 FSM_ENABLE (1Ah) . . . 72
10.16 FSM_LONG_COUNTER_L (1Ch) and FSM_LONG_COUNTER_H (1Dh) . . . 72
10.17 INT_ACK_MASK (1Fh) . . . 73
10.18 FSM_OUTS1 (20h) . . . 74
10.19 FSM_OUTS2 (21h) . . . 74
10.20 FSM_OUTS3 (22h) . . . 75
10.21 FSM_OUTS4 (23h) . . . 75
10.22 FSM_OUTS5 (24h) . . . 76
10.23 FSM_OUTS6 (25h) . . . 76
10.24 FSM_OUTS7 (26h) . . . 77
10.25 FSM_OUTS8 (27h) . . . 77
10.26 STEP_COUNTER_L (28h) and STEP_COUNTER_H (29h) . . . 78
10.27 EMB_FUNC_SRC (2Ah) . . . 78
10.28 EMB_FUNC_INIT_A (2Ch) . . . 79
10.29 EMB_FUNC_INIT_B (2Dh) . . . 79
10.30 MLC1_SRC (34h) . . . 79
10.31 MLC2_SRC (35h) . . . 80

10.32 MLC3_SRC (36h) . . . 80
10.33 MLC4_SRC (37h) . . . 80
10.34 FSM_ODR (39h) . . . 81
10.35 MLC_ODR (3Ah) . . . 82
11 Embedded advanced features pages . . . 83
12 Embedded advanced features register description . . . 85
12.1 Page 0 - embedded advanced features registers . . . 85
12.1.1 FSM_LC_TIMEOUT_L (54h) and FSM_LC_TIMEOUT_H (55h) . . . 85
12.1.2 FSM_PROGRAMS (56h) . . . 85
12.1.3 FSM_START_ADD_L (58h) and FSM_START_ADD_H (59h) . . . 86
12.1.4 PEDO_CMD_REG (5Dh) . . . 86
12.1.5 PEDO_DEB_STEPS_CONF (5Eh) . . . 87
12.1.6 PEDO_SC_DELTAT_L (AAh) and PEDO_SC_DELTAT_H (ABh) . . . 87
12.1.7 AH_BIO_SENSITIVITY_L (B6h) and AH_BIO_SENSITIVITY_H (B7h) . . . 88
12.1.8 SMART_POWER_CTRL (D2h) . . . 88
13 Package information . . . 89
13.1 Soldering information . . . 89
13.2 LGA-12L package information . . . 89
13.3 LGA-12L packing information . . . 90
Revision history . . . 92
List of tables . . . 98
List of figures . . . 103

List of tables

Table 1. Pin description . . . 4
Table 2. Configuration of duration of interrupt . . . 8
Table 3. Electrical parameters of analog hub / vAFE (@VDD = 1.8 V, T = 25°C) . . . 9
Table 4. Electrical characteristics . . . 10
Table 5. Mechanical characteristics . . . 11
Table 6. SPI target timing values . . . 12
Table 7. I²C target timing values . . . 14
Table 8. Absolute maximum ratings . . . 15
Table 9. Serial interface pin description . . . 17
Table 10. I²C terminology . . . 17
Table 11. TAD+read/write patterns . . . 18
Table 12. Transfer when controller is writing one byte to target . . . 18
Table 13. Transfer when controller is writing multiple bytes to target . . . 18
Table 14. Transfer when controller is receiving (reading) one byte of data from target . . . 18
Table 15. Transfer when controller is receiving (reading) multiple bytes of data from target . . . 18
Table 16. MIPI I3C® CCC commands . . . 23
Table 17. Internal pin status . . . 26
Table 18. Register map . . . 34
Table 19. Table 20. EXT_CLK_CFG register . . . 36
Table 20. EXT_CLK_CFG register description . . . 36
Table 21. Table 20. PIN_CTRL register . . . 36
Table 22. PIN_CTRL register description . . . 36
Table 23. WAKE_UP_DUR_EXT register . . . 37
Table 24. WAKE_UP_DUR_EXT register description . . . 37
Table 25. WHO_AM_I register default values . . . 37
Table 26. CTRL1 register . . . 37
Table 27. CTRL1 register description . . . 37
Table 28. CTRL2 register . . . 38
Table 29. CTRL2 register description . . . 38
Table 30. CTRL3 register . . . 38
Table 31. CTRL3 register description . . . 38
Table 32. CTRL4 register . . . 39
Table 33. CTRL4 register description . . . 39
Table 34. ODR frequency in inactivity state . . . 39
Table 35. CTRL5 register . . . 40
Table 36. CTRL5 register description . . . 40
Table 37. Operating modes . . . 40
Table 38. Bandwidth selection (low-power mode with ODR < 50 Hz) . . . 41
Table 39. Output data rate / bandwidth configurations in AH / vAFE only state . . . 41
Table 40. Full-scale selection . . . 41
Table 41. FIFO_CTRL register description . . . 42
Table 42. Selection of FIFO mode . . . 42
Table 43. FIFO_WTM register . . . 43
Table 44. FIFO_WTM register description . . . 43
Table 45. INTERRUPT_CFG register . . . 43
Table 46. INTERRUPT_CFG register description . . . 43
Table 47. SIXD register . . . 44
Table 48. SIXD register description . . . 44
Table 49. WAKE_UP_THS register . . . 44
Table 50. WAKE_UP_THS register description . . . 44
Table 51. WAKE_UP_DUR register . . . 45
Table 52. WAKE_UP_DUR register description . . . 45
Table 53. FREE_FALL register . . . 45

Table 54. FREE_FALL register description . . . 45
Table 55. MD1_CFG register . . . 46
Table 56. MD1_CFG register description . . . 46
Table 57. WAKE_UP_SRC register . . . 47
Table 58. WAKE_UP_SRC register description . . . 47
Table 59. TAP_SRC register . . . 48
Table 60. TAP_SRC register description . . . 48
Table 61. SIXD_SRC register . . . 48
Table 62. SIXD_SRC register description . . . 48
Table 63. ALL_INT_SRC register . . . 49
Table 64. ALL_INT_SRC register description . . . 49
Table 65. STATUS register . . . 49
Table 66. STATUS register description . . . 49
Table 67. FIFO_STATUS1 register . . . 50
Table 68. FIFO_STATUS1 register description . . . 50
Table 69. FIFO_STATUS2 register . . . 50
Table 70. FIFO_STATUS2 register description . . . 50
Table 71. OUT_X_L register . . . 50
Table 72. OUT_X_L register description . . . 50
Table 73. OUT_X_H register . . . 50
Table 74. OUT_X_H register description . . . 50
Table 75. OUT_Y_L register . . . 51
Table 76. OUT_Y_L register description . . . 51
Table 77. OUT_Y_H register . . . 51
Table 78. OUT_Y_H register description . . . 51
Table 79. OUT_Z_L register . . . 51
Table 80. OUT_Z_L register description . . . 51
Table 81. OUT_Z_H register . . . 51
Table 82. OUT_Z_H register description . . . 51
Table 83. OUT_AH_BIO_L register . . . 52
Table 84. OUT_AH_BIO_L register description . . . 52
Table 85. OUT_AH_BIO_H register . . . 52
Table 86. OUT_AH_BIO_H register description . . . 52
Table 87. AH_BIO_CFG1 register . . . 52
Table 88. AH_BIO_CFG1 register description . . . 52
Table 89. AH_BIO_CFG2 register . . . 53
Table 90. AH_BIO_CFG2 register description . . . 53
Table 91. AH_BIO_CFG3 register . . . 54
Table 92. AH_BIO_CFG3 register description . . . 54
Table 93. I3C_IF_CTRL register . . . 54
Table 94. I3C_IF_CTRL register description . . . 54
Table 95. EMB_FUNC_STATUS_MAINPAGE register . . . 54
Table 96. EMB_FUNC_STATUS_MAINPAGE register description . . . 54
Table 97. FSM_STATUS_MAINPAGE register . . . 55
Table 98. FSM_STATUS_MAINPAGE register description . . . 55
Table 99. MLC_STATUS_MAINPAGE register . . . 55
Table 100. MLC_STATUS_MAINPAGE register description . . . 55
Table 101. EN_DEVICE_CONFIG register . . . 55
Table 102. EN_DEVICE_CONFIG register description . . . 55
Table 103. FUNC_CFG_ACCESS register . . . 56
Table 104. FUNC_CFG_ACCESS register description . . . 56
Table 105. FIFO_DATA_OUT_TAG register . . . 56
Table 106. FIFO_DATA_OUT_TAG register description . . . 56
Table 107. Identification of sensor in FIFO . . . 56
Table 108. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L registers . . . 57

Table 109. FIFO_DATA_OUT_X_H and FIFO_DATA_OUT_X_L register description . . . 57
Table 110. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L registers . . . 57
Table 111. FIFO_DATA_OUT_Y_H and FIFO_DATA_OUT_Y_L register description . . . 57
Table 112. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L registers . . . 57
Table 113. FIFO_DATA_OUT_Z_H and FIFO_DATA_OUT_Z_L register description . . . 57
Table 114. FIFO_BATCH_DEC register . . . 58
Table 115. FIFO_BATCH_DEC register description . . . 58
Table 116. Accelerometer batch data rate . . . 58
Table 117. TAP_CFG0 register . . . 59
Table 118. TAP_CFG0 register description . . . 59
Table 119. TAP_CFG1 register . . . 59
Table 120. TAP_CFG1 register description . . . 59
Table 121. TAP_CFG2 register . . . 60
Table 122. TAP_CFG2 register description . . . 60
Table 123. TAP_CFG3 register . . . 60
Table 124. TAP_CFG3 register description . . . 60
Table 125. TAP_CFG4 register . . . 60
Table 126. TAP_CFG4 register description . . . 60
Table 127. TAP_CFG5 register . . . 61
Table 128. TAP_CFG5 register description . . . 61
Table 129. TAP_CFG6 register . . . 61
Table 130. TAP_CFG6 register description . . . 61
Table 131. TIMESTAMP output registers . . . 62
Table 132. TIMESTAMP output register description . . . 62
Table 133. Register address map - embedded functions . . . 63
Table 134. PAGE_SEL register . . . 65
Table 135. PAGE_SEL register description . . . 65
Table 136. EMB_FUNC_EN_A register . . . 65
Table 137. EMB_FUNC_EN_A register description . . . 65
Table 138. EMB_FUNC_EN_B register . . . 66
Table 139. EMB_FUNC_EN_B register description . . . 66
Table 140. EMB_FUNC_EXEC_STATUS register . . . 66
Table 141. EMB_FUNC_EXEC_STATUS register description . . . 66
Table 142. PAGE_ADDRESS register . . . 66
Table 143. PAGE_ADDRESS register description . . . 66
Table 144. PAGE_VALUE register . . . 67
Table 145. PAGE_VALUE register description . . . 67
Table 146. EMB_FUNC_INT register . . . 67
Table 147. EMB_FUNC_INT register description . . . 67
Table 148. FSM_INT register . . . 68
Table 149. FSM_INT register description . . . 68
Table 150. MLC_INT register . . . 69
Table 151. MLC_INT register description . . . 69
Table 152. EMB_FUNC_STATUS register . . . 69
Table 153. EMB_FUNC_STATUS register description . . . 69
Table 154. FSM_STATUS register . . . 70
Table 155. FSM_STATUS register description . . . 70
Table 156. MLC_STATUS register . . . 70
Table 157. MLC_STATUS register description . . . 70
Table 158. PAGE_RW register . . . 71
Table 159. PAGE_RW register description . . . 71
Table 160. EMB_FUNC_FIFO_EN register . . . 71
Table 161. EMB_FUNC_FIFO_EN register description . . . 71
Table 162. FSM_ENABLE register . . . 72
Table 163. FSM_ENABLE register description . . . 72

Table 164. FSM_LONG_COUNTER_L register . . . 72
Table 165. FSM_LONG_COUNTER_L register description . . . 72
Table 166. FSM_LONG_COUNTER_H register . . . 72
Table 167. FSM_LONG_COUNTER_H register description . . . 72
Table 168. INT_ACK_MASK register . . . 73
Table 169. INT_ACK_MASK register description . . . 73
Table 170. FSM_OUTS1 register . . . 74
Table 171. FSM_OUTS1 register description . . . 74
Table 172. FSM_OUTS2 register . . . 74
Table 173. FSM_OUTS2 register description . . . 74
Table 174. FSM_OUTS3 register . . . 75
Table 175. FSM_OUTS3 register description . . . 75
Table 176. FSM_OUTS4 register . . . 75
Table 177. FSM_OUTS4 register description . . . 75
Table 178. FSM_OUTS5 register . . . 76
Table 179. FSM_OUTS5 register description . . . 76
Table 180. FSM_OUTS6 register . . . 76
Table 181. FSM_OUTS6 register description . . . 76
Table 182. FSM_OUTS7 register . . . 77
Table 183. FSM_OUTS7 register description . . . 77
Table 184. FSM_OUTS8 register . . . 77
Table 185. FSM_OUTS8 register description . . . 77
Table 186. STEP_COUNTER_L register . . . 78
Table 187. STEP_COUNTER_L register description . . . 78
Table 188. STEP_COUNTER_H register . . . 78
Table 189. STEP_COUNTER_H register description . . . 78
Table 190. EMB_FUNC_SRC register . . . 78
Table 191. EMB_FUNC_SRC register description . . . 78
Table 192. EMB_FUNC_INIT_A register . . . 79
Table 193. EMB_FUNC_INIT_A register description . . . 79
Table 194. EMB_FUNC_INIT_B register . . . 79
Table 195. EMB_FUNC_INIT_B register description . . . 79
Table 196. MLC1_SRC register . . . 79
Table 197. MLC1_SRC register description . . . 79
Table 198. MLC2_SRC register . . . 80
Table 199. MLC2_SRC register description . . . 80
Table 200. MLC3_SRC register . . . 80
Table 201. MLC3_SRC register description . . . 80
Table 202. MLC4_SRC register . . . 80
Table 203. MLC4_SRC register description . . . 80
Table 204. FSM_ODR register . . . 81
Table 205. FSM_ODR register description . . . 81
Table 206. MLC_ODR register . . . 82
Table 207. MLC_ODR register description . . . 82
Table 208. Register address map - embedded advanced features page 0 . . . 83
Table 209. FSM_LC_TIMEOUT_L register . . . 85
Table 210. FSM_LC_TIMEOUT_L register description . . . 85
Table 211. FSM_LC_TIMEOUT_H register . . . 85
Table 212. FSM_LC_TIMEOUT_H register description . . . 85
Table 213. FSM_PROGRAMS register . . . 85
Table 214. FSM_PROGRAMS register description . . . 85
Table 215. FSM_START_ADD_L register . . . 86
Table 216. FSM_START_ADD_L register description . . . 86
Table 217. FSM_START_ADD_H register . . . 86
Table 218. FSM_START_ADD_H register description . . . 86

Table 219. PEDO_CMD_REG register . . . 86
Table 220. PEDO_CMD_REG register description . . . 86
Table 221. PEDO_DEB_STEPS_CONF register . . . 87
Table 222. PEDO_DEB_STEPS_CONF register description . . . 87
Table 223. PEDO_SC_DELTAT_L register . . . 87
Table 224. PEDO_SC_DELTAT_H register . . . 87
Table 225. PEDO_SC_DELTAT_H/L register description . . . 87
Table 226. AH_BIO_SENSITIVITY_L register . . . 88
Table 227. AH_BIO_SENSITIVITY_L register description . . . 88
Table 228. AH_BIO_SENSITIVITY_H register . . . 88
Table 229. AH_BIO_SENSITIVITY_H register description . . . 88
Table 230. SMART_POWER_CTRL register . . . 88
Table 231. SMART_POWER_CTRL register description . . . 88
Table 232. Reel dimensions for carrier tape of LGA-12L package . . . 91
Table 233. Document revision history . . . 92

List of figures

Figure 1. Block diagram . . . 3
Figure 2. Pin connections . . . 4
Figure 3. SPI target timing in mode 0 . . . 12
Figure 4. SPI target timing in mode 3 . . . 13
Figure 5. I²C target timing diagram . . . 14
Figure 6. Read and write protocol . . . 19
Figure 7. SPI read protocol . . . 20
Figure 8. Multiple byte SPI read protocol (2-byte example) . . . 20
Figure 9. SPI write protocol . . . 21
Figure 10. Multiple byte SPI write protocol (2-byte example) . . . 21
Figure 11. SPI read protocol in 3-wire mode . . . 21
Figure 12. ST1VAFE3BX electrical connections (top view) . . . 25
Figure 13. vAFE external connections to pin 11, 12 (vAFE input) . . . 25
Figure 14. Four-stage pedometer algorithm . . . 30
Figure 15. Generic state machine . . . 31
Figure 16. State machine in the ST1VAFE3BX . . . 32
Figure 17. Machine learning core in the ST1VAFE3BX . . . 32
Figure 18. LGA-12L 2.0 x 2.0 x 0.74 mm package outline and mechanical data . . . 89
Figure 19. Carrier tape information for LGA-12L package . . . 90
Figure 20. LGA-12L package orientation in carrier tape . . . 90
Figure 21. Reel information for carrier tape of LGA-12L package . . . 91

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved