ATF750C(L) 5V 10-Macrocell CPLD Data Sheet

Features

- High-Speed, Electrically-Erasable Complex Programmable Logic Device:
  - Superset of 22V10
  - Enhanced logic flexibility
  - Backward Compatible with ATV750B/BL and ATV750/L
- Edge-sensing automatic 1 mA Standby (ATF750CL)
- D- or T-type Flip-flop
- Product Term or Direct Input Pin Clocking for Flip-flop
- 7.5 ns Maximum Pin-to-pin Delay with 5V Operation
- Highest Density Programmable Logic Available in 24-pin and 28-pin Packages
- Increased Logic Flexibility
  - 42 array inputs, 20 sum terms and 20 flip-flops
- Enhanced Output Logic Flexibility
  - All 20 flip-flops feedback internally
  - 10 flip-flops are also available as outputs
- Programmable pin-keeper circuits on inputs and I/Os
- Dual-in-line and Surface Mount Packages in Standard Pinouts
- Available in Military, Commercial and Industrial Temperature Ranges
- Robust EEPROM Technology:
  - 100% tested
  - Completely reprogrammable
  - 1,000 Program/Erase cycles
  - 20-year data retention
  - 2000V ESD protection
- Security Fuse Feature
- Green (Pb/Halide-Free/RoHS Compliant) Package Options

Packages

- 24-Lead CerDIP
- 24-Lead PDIP
- 24-Lead SOIC
- 24-Lead TSSOP
- 28-Lead CLCC
- 28-Lead PLCC

Description

The ATF750C(L) is a high-performance, complex programmable logic device (CPLD) that utilizes Microchip's proven electrically-erasable memory technology. The ATF750C(L) is twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations translate into more usable gates. High-speed logic and uniform predictable delays guarantee fast in-system performance.

Each of the ATF750C(L)'s 22 logic pins can be used as an input. Ten of these can be used as inputs, outputs or bi-directional I/O pins. Each flip-flop is individually configurable as either D- or T-type. Each flip-flop output is fed back into the array independently. This allows burying of all the sum terms and flip-flops.

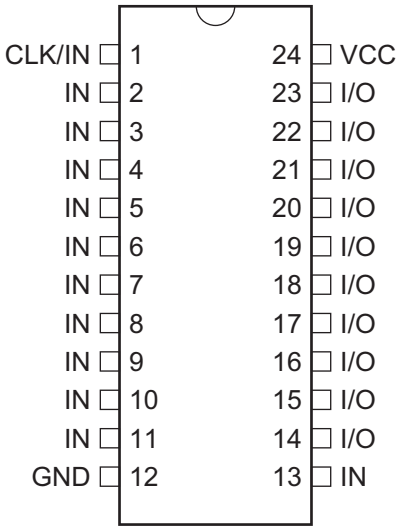
There are 171 total product terms available. There are two sum terms per output, providing added flexibility. A variable format is used to assign between four to eight product terms per sum term. Much more logic can be replaced by this device than by any other 24-pin PLD. With 20 sum terms and flip-flops, complex state machines are easily implemented with logic to spare.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

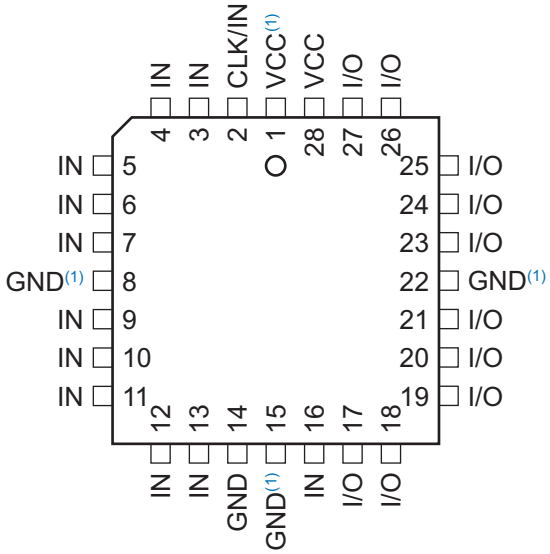
The ATF750CL is a low-power device with speeds as fast as 15 ns. The ATF750CL provides the optimum low-power CPLD solution. This device significantly reduces total system power, thereby allowing battery-powered operations.

Pin Configurations and Pinouts

24-Lead CerDIP/PDIP/SOIC/TSSOP
(Top View)

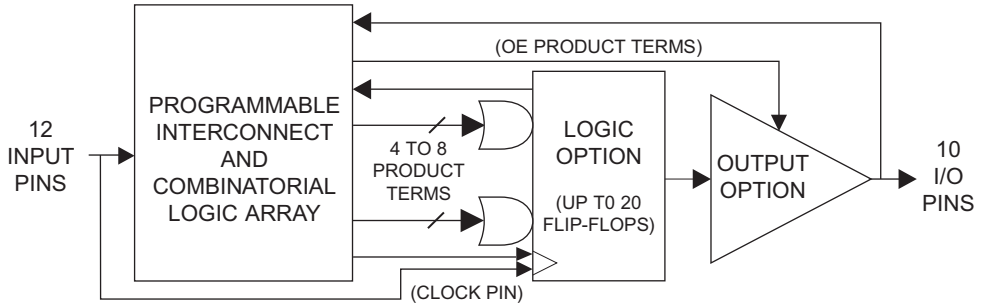


28-Lead PLCC/CLCC
(Top View)



Note 1: For PLCC/CLCC, pins 1, 8, 15, and 22 can be left unconnected. For superior performance, connect VCC to pin 1 and GND to pins 8, 15, and 22.

Block Diagram



The ATF750C(L)'s advanced flexibility packs more usable gates into 24 pins than any other logic device. The ATF750C(L) starts with the popular 22V10 architecture, and add several enhanced features:

Selectable D- and T-type Registers

Each ATF750C(L) flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.

Selectable Asynchronous Clocks

Each of the ATF750C(L)'s flip-flops may be clocked by its own clock product term or directly from Pin 1 (Pin 2 for PLCC/CLCC). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.

A Full Bank of Ten More Registers

The ATF750C(L) provides two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.

Independent I/O Pin and Feedback Paths

Each I/O pin on the ATF750C(L) has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature, combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

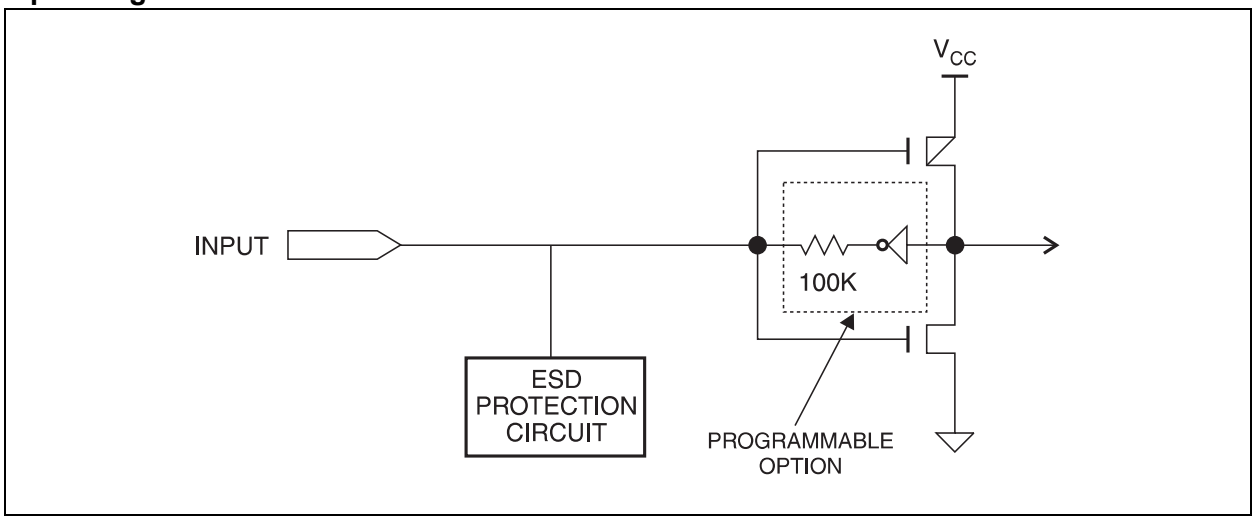
Bus-Friendly Pin-Keeper Input and I/Os

All input and I/O pins on the ATF750C(L) have programmable "pin-keeper" circuits. If activated, when any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level.

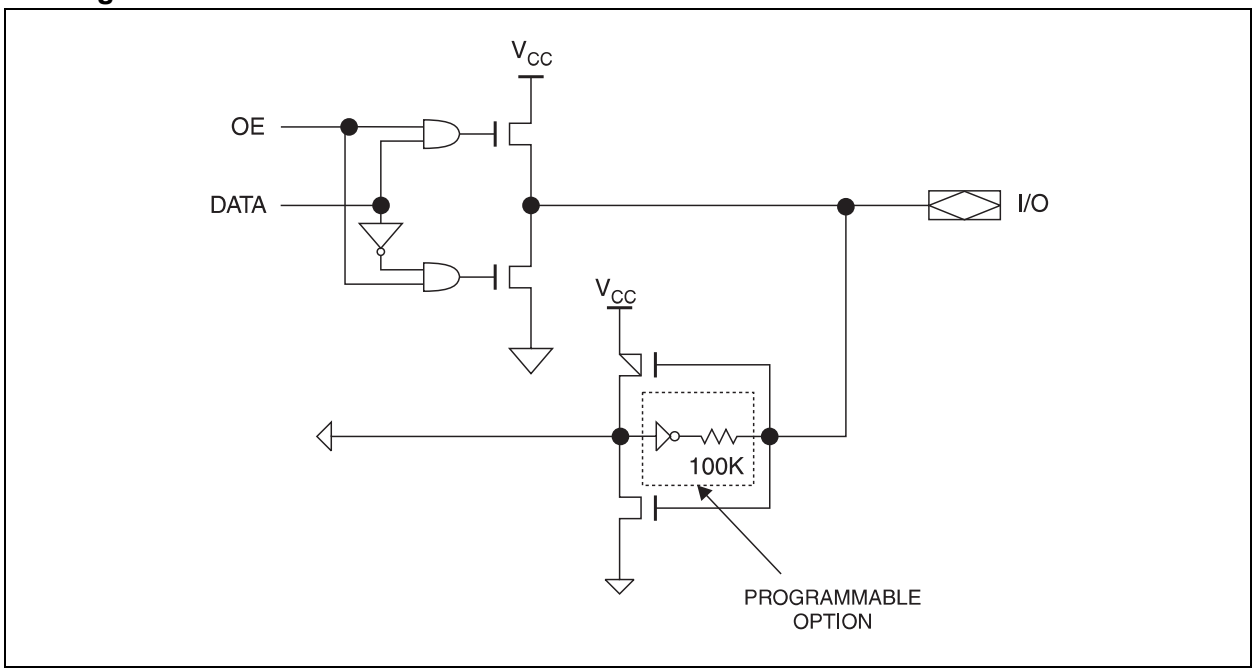
This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Enabling or disabling of the pin-keeper circuits is controlled by the device type chosen in the logic compiler device selection menu. Please refer to the software compiler table for more details. Once the pin-keeper circuits are disabled, normal termination procedures are required for unused inputs and I/Os.

Input Diagram



I/O Diagram



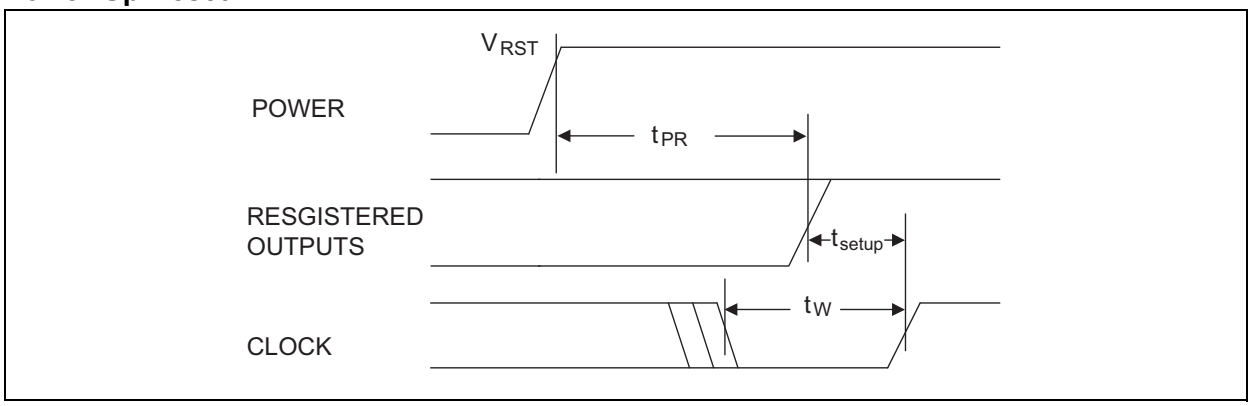
Power-Up Reset

The registers in ATF750C(L) are to reset during power-up. At a point delayed slightly from VCC crossing VRST, all registers will be reset to the low state. The output state will depend on the polarity of its buffer.

The feature is critical for state machine initialization. However, due to the asynchronous nature of Reset and uncertainty of how VCC actually rises in the system, the following conditions are required:

- The VCC rise must be monotonic
- After Reset occurs, all input and feedback setup times must be met before driving the clock pin high
- The clock must remain stable during Power-up Reset

Power-Up Reset



Power-Up Reset Parameters

Parameter	Description	Typ.	Max.	Units
tPR	Power-Up Reset Time	600	1000	ns
VRST	Power-Up Reset Voltage	2.0	4.5	V

Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATF750C(L). The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both the Q0 and Q1 flip-flops are reset when the input signals received force the internal resets high.

Software Support

All family members of the ATF750C(L) can be designed with Microchip's WinCUPL software tool.

Additionally, the ATF750C(L) may be programmed to perform the ATV750(L) functional subset (no T-type flip-flops, pin clocking or D/T2 feedback) using the ATV750(L) JEDEC file. In this case, the ATF750C(L) becomes a direct replacement or speed upgrade for the ATV750(L). The ATF750C(L) is a direct replacement for the ATV750(L) and the ATV750B(L).

Software Compiler Mode Selection

Device	WinCUPL Device Mnemonic	Pin-keeper
ATF750C(L) CerDIP/PDIP/SOIC /TSSOP	V750C V750CPPK	Disabled Enabled
ATF750C(L) PLCC/CLCC	V750LCC V750CPPKLCC	Disabled Enabled

Third Party Programmer Support

Device	Description
ATF750C (V750)	**V750 Cross-programming.** JEDEC file compatible with standard V750 JEDEC file (total fuses in JEDEC file = 14394). The Programmer will automatically program "0"s into the User Row (UES), and disable the Pin-keeper features. The Fuse Checksum will be the same as the old ATV750(L) file. This device type is recommended for customers that are directly migrating from an ATV750(L) device to an ATF750C(L) device.
ATF750C (V750B)	**V750B Cross-programming.** JEDEC file compatible with standard V750B JEDEC file (total fuses in JEDEC file = 14435). The Programmer will automatically program "0"s into the User Row (UES), and disable the Pin-keeper feature. The Fuse Checksum will be the same as the old ATV750B(L) file. This device type is recommended for customers that are directly migrating from an ATV750B(L) device to an ATF750C(L) device.
ATF750C	Programming of User Row (UES) bits supported and Pin-keeper bit is user programmable. (Total fuses in JEDEC file = 14504). This is the default device type and is recommended for users that have re-compiled their source design files to specifically target the ATF750C(L) device.

Note: The ATF750C(L) has 14,504 JEDEC fuses.

Security Fuse Usage

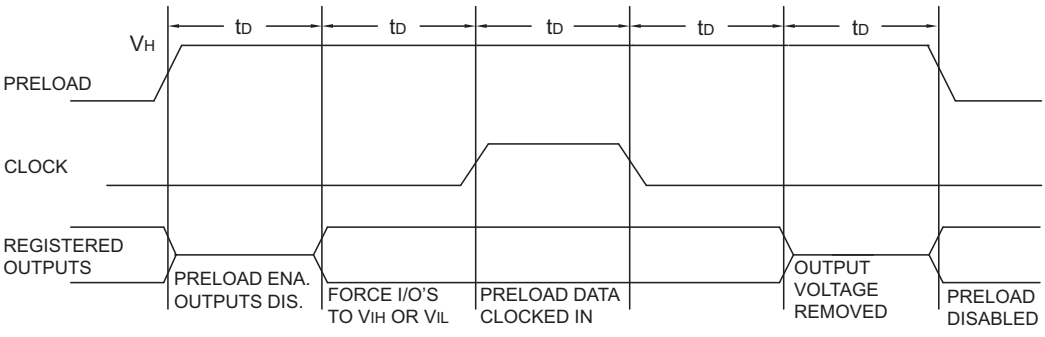
A single fuse is provided to prevent unauthorized copying of the ATF750C(L) fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

Preload of Registered Outputs

The ATF750C(L)'s registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the output polarity. The PRELOAD state is entered by placing a 10.25V to 10.75V signal on pin 8 (pin 20 for PLCC/CLCC). When the clock term is pulsed high, the data on the I/O pins is placed into the register chosen by the select pin.

Preload of Registered Outputs



Level Forced on Registered Output Pin during Preload Cycles	Select Pin State	Register #0 State after Cycle	Register #1 State after Cycle
V_{IH}	Low	High	X
V_{IL}	Low	Low	X
V_{IH}	High	X	High
V_{IL}	High	X	Low

1.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -55°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to ground(1) ..... -2.0V to +7.0V

Voltage on input pins with respect to ground during programming(1) ..... -2.0V to +14.0V

Programming voltage with respect to ground(1) ..... -2.0V to +14.0V

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

TABLE 1-1: DC AND AC OPERATING CONDITIONS

	Commercial	Industrial	Military
Operating Temperature (Ambient)	0°C to +70°C	-40°C to +85°C	-55°C to +125°C (case)
V_{CC} Power Supply	5V ± 5%	5V ± 10%	5V ± 10%

TABLE 1-2: DC CHARACTERISTICS

Symbol	Parameter	Minimum	Typical	Maximum	Units	Condition		
I_{LI}	Input Leakage Current	—	—	10	µA	V_{IN} = -0.1V to V_{CC} + 1V		
I_{LO}	Output Leakage Current	—	—	10	µA	V_{OUT} = -0.1V to V_{CC} + 0.1V		
I_{CC}	Power Supply Current, Standby	—	125	180	mA	Comm.	Std mode	V_{CC} = Max, V_{IN} = Max, Outputs Open
		—	135	190	mA	Ind., Mil.		
		—	0.12	1	mA	Comm.	"L" mode	
		—	0.15	2	mA	Ind., Mil.		
I_{OS}(1)	Output Short Circuit Current	—	—	-120	mA	V_{OUT} = 0.5V		
V_{IL}	Input Low Voltage	-0.6	—	0.8	V	4.5 ≤ V_{CC} ≤ 5.5V		
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.75	V			
V_{OL}	Output Low Voltage	—	—	0.5	V	Comm., Ind.	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min, I_{OL} = 16 mA	
		—	—	0.5	V	Mil,	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min, I_{OL} = 12 mA	
		—	—	0.8	V	Comm.	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min, I_{OL} = 24 mA	
V_{OH}	Output High Voltage	2.4	—	—	V	V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min, I_{OH} = -4.0 mA		

Note 1: Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

TABLE 1-3: PIN CAPACITANCE

	Typical	Maximum	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V; f = 1.0 MHz; T_A = 25°C(1)
$C_{I/O}$	6	8	pF	V_{OUT} = 0V; f = 1.0 MHz; T_A = 25°C(1)

Note 1: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

TABLE 1-4: AC CHARACTERISTICS, PRODUCT TERM CLOCK

Symbol	Parameter	-7		-10		C/CL-15		Units
		Min.	Max.	Min.	Max.			
t_{PD}	Input or Feedback to Non-Registered Output	—	7.5	—	10	—	15	ns
t_{EA}	Input to Output Enable	—	7.5	—	10	—	15	ns
t_{ER}	Input to Output Disable	—	7.5	—	10	—	15	ns
t_{CO}	Clock to Output	3	7.5	4	10	5	12	ns
t_{CF}	Clock to Feedback	1	5	4	7.5	5	9	ns
t_S	Input Setup Time	3	—	4	—	8/12	—	ns
t_{SF}	Feedback Setup Time	3	—	4	—	7	—	ns
t_H	Hold Time	1	—	2	—	5	—	ns
t_P	Clock Period	7	—	11	—	14	—	ns
t_W	Clock Width	3.5	—	5.5	—	7	—	ns
f_{MAX}	External Feedback 1/(t_S + t_{CO})	—	95	—	71	—	50/41	MHz
	Internal Feedback 1/(t_{SF} + t_{CF})	—	125	—	86	—	62	MHz
	No Feedback 1/(t_P)	—	142	—	90	—	71	MHz
t_{AW}	Asynchronous Reset Width	5	—	10	—	15	—	ns
t_{AR}	Asynchronous Reset Recovery Time	3	—	10	—	15	—	ns
t_{AP}	Asynchronous Reset to Registered Output Reset	—	8	—	12	—	15	ns
t_{SP}	Setup Time, Synchronous Preset	4	—	7	—	8	—	ns

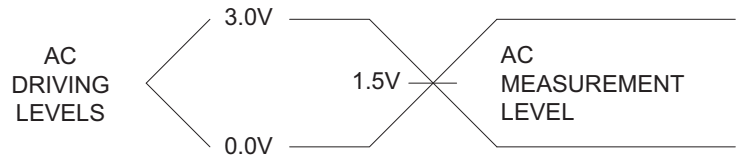
TABLE 1-5: AC CHARACTERISTICS, INPUT PIN CLOCK

Symbol	Parameter	-7		-10		C/CL-15		Units
		Min.	Max.	Min.	Max.			
t_{PD}	Input or Feedback to Non-registered Output	—	7.5	—	10	—	15	ns
t_{EA}	Input to Output Enable	—	7.5	—	10	—	15	ns
t_{ER}	Input to Output Disable	—	7.5	—	10	—	15	ns
t_{COS}	Clock to Output	0	6.5	0	7	0	10	ns
t_{CFS}	Clock to Feedback	0	3.5	0	5	0	5.5	ns
t_{SS}	Input Setup Time	4	—	5	—	8/12.5	—	ns
t_{SFS}	Feedback Setup Time	4	—	5	—	7	—	ns

TABLE 1-5: AC CHARACTERISTICS, INPUT PIN CLOCK

Symbol	Parameter	-7		-10		C/CL-15		Units
		Min.	Max.	Min.	Max.			
t_{HS}	Hold Time	0	—	0	—	0	—	ns
t_{PS}	Clock Period	7	—	10	—	12	—	ns
t_{WS}	Clock Width	3.5	—	5	—	6	—	ns
f_{MAXS}	External Feedback 1/(t_{SS} + t_{COS})	—	95	—	83	—	55/44	MHz
	Internal Feedback 1/(t_{SFS} + t_{CFS})	—	133	—	100	—	80	MHz
	No Feedback 1/(t_{PS})	—	142	—	100	—	83	MHz
t_{AW}	Asynchronous Reset Width	5	—	10	—	15	—	ns
t_{ARS}	Asynchronous Reset Recovery Time	5	—	10	—	15	—	ns
t_{AP}	Asynchronous Reset to Registered Output Reset	—	8	—	10	—	15	ns
t_{SPS}	Setup Time, Synchronous Preset	5	—	5/9	—	11	—	ns

FIGURE 1-1: INPUT TEST WAVEFORMS AND MEASUREMENT LEVELS



Note: t_R, t_F < 3 ns (10% to 90%)

FIGURE 1-2: OUTPUT AC TEST LOADS

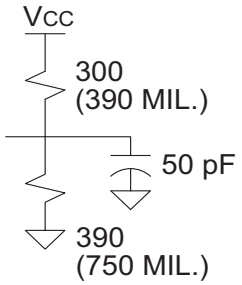
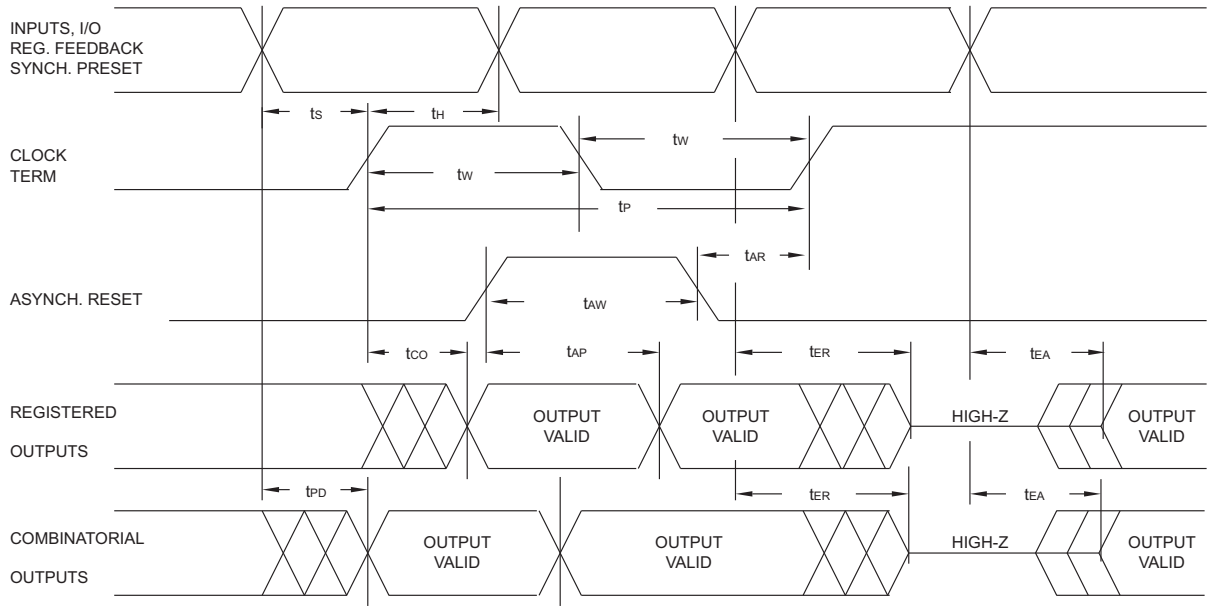
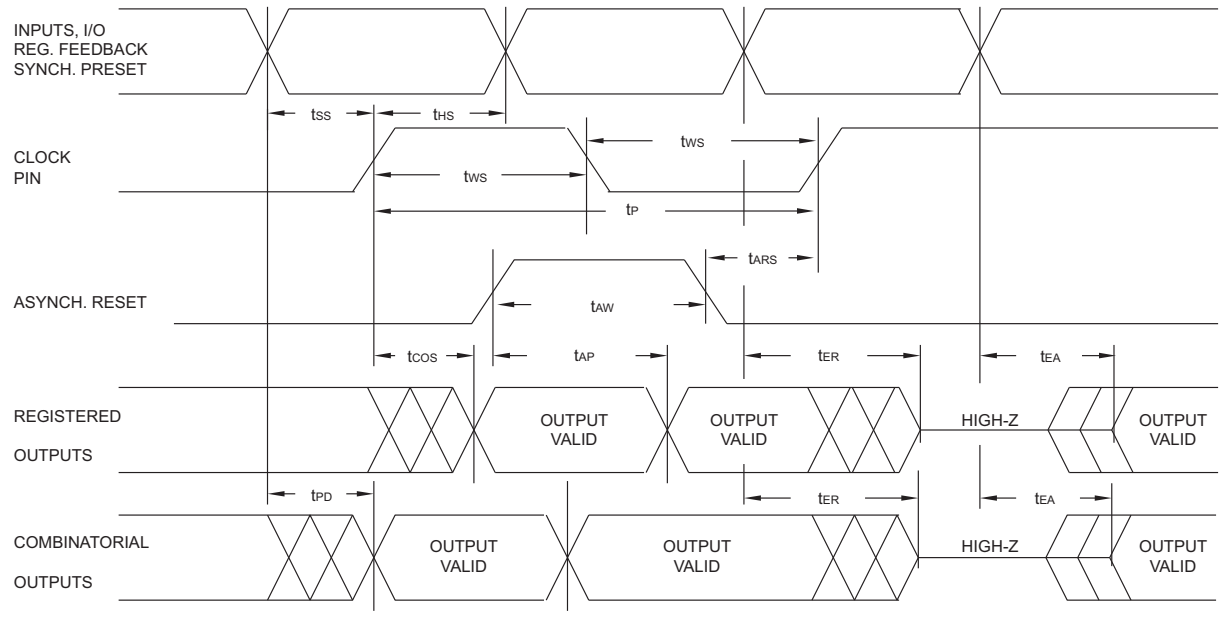


FIGURE 1-3: AC WAVEFORMS, PRODUCT TERM CLOCK



Note: Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

FIGURE 1-4: AC WAVEFORMS, INPUT PIN CLOCK



Note: Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

2.0 PINOUTS

TABLE 2-1: DEDICATED PINOUTS

Dedicated Pin	24-Lead CerDIP/PDIP/SOIC/TSSOP	28-Lead CLCC/PLCC
CLK/IN	1	2
IN	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13	3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 16
GND(1)	12,	8, 14, 15, 22
I/O	14, 15, 16, 17, 18, 19, 20, 21, 22, 23	17, 18, 19, 20, 21, 23, 24, 25, 26, 27
VCC(2)	24	1, 28

Note 1: GND = Ground pins

2: VCC = +5V supply pins for the device

3.0 LOGIC OPTIONS

FIGURE 3-1: COMBINATORIAL OUTPUT

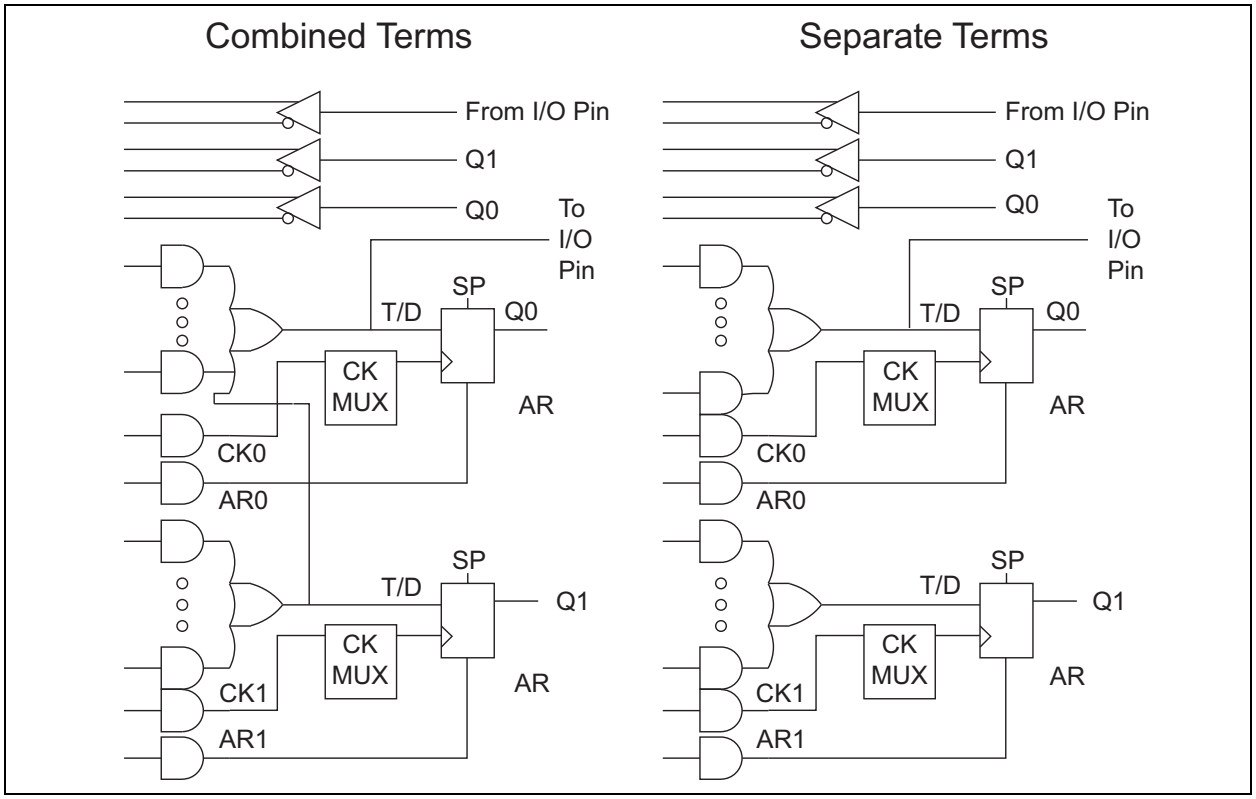
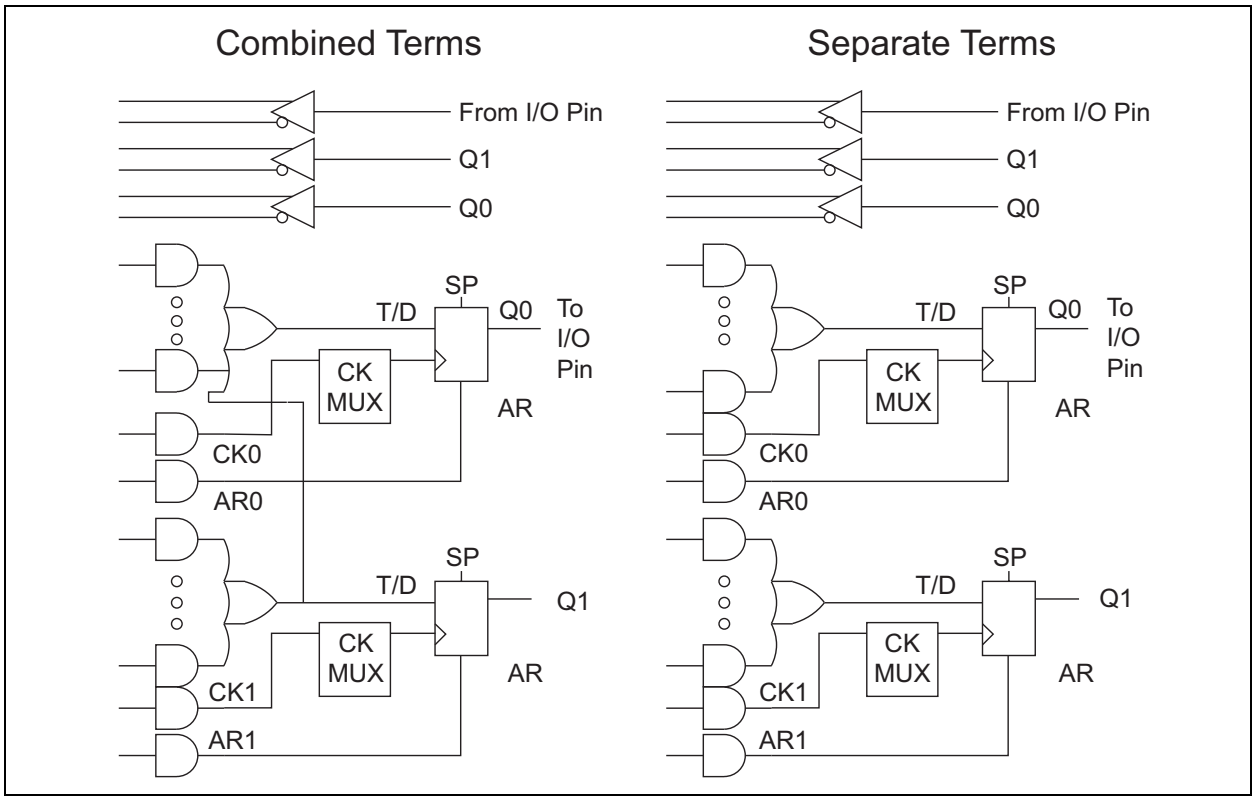
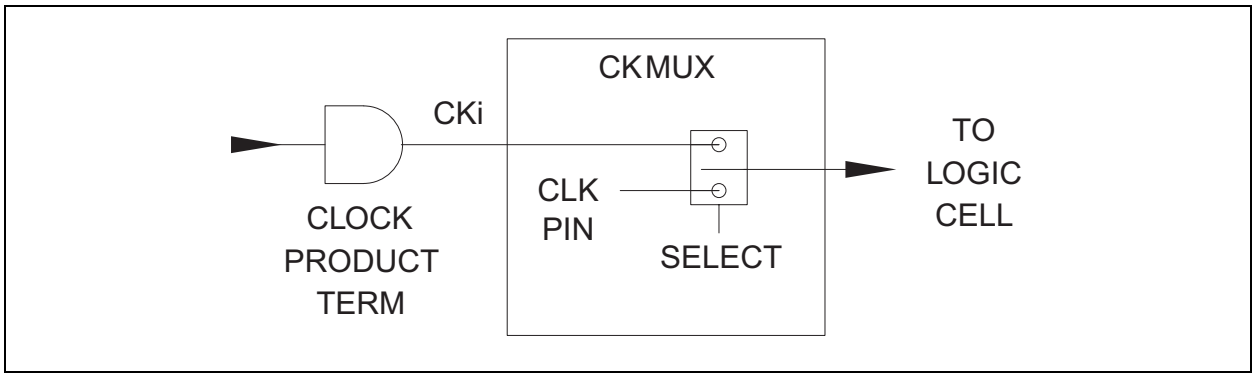


FIGURE 3-2: REGISTERED OUTPUT



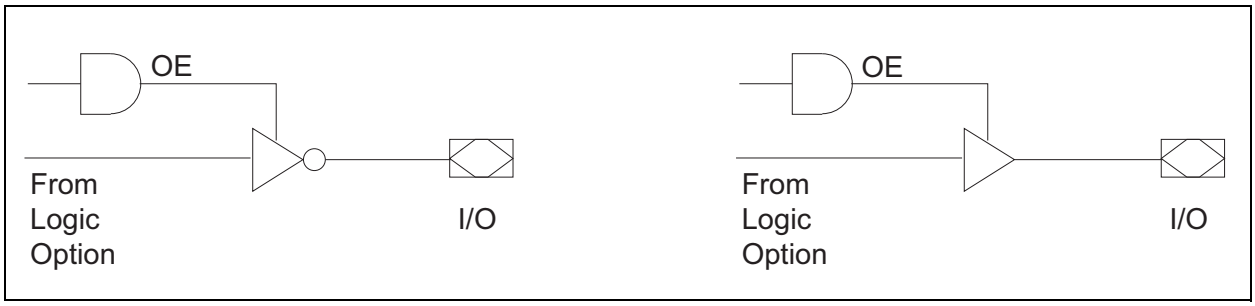
4.0 CLOCK OPTIONS

FIGURE 4-1: CLOCK MUX



5.0 OUTPUT OPTIONS

FIGURE 5-1: OUTPUT OPTIONS



6.0 FUNCTIONAL LOGIC DIAGRAMS

FIGURE 6-1: FUNCTIONAL LOGIC DIAGRAM ATF750C, UPPER HALF

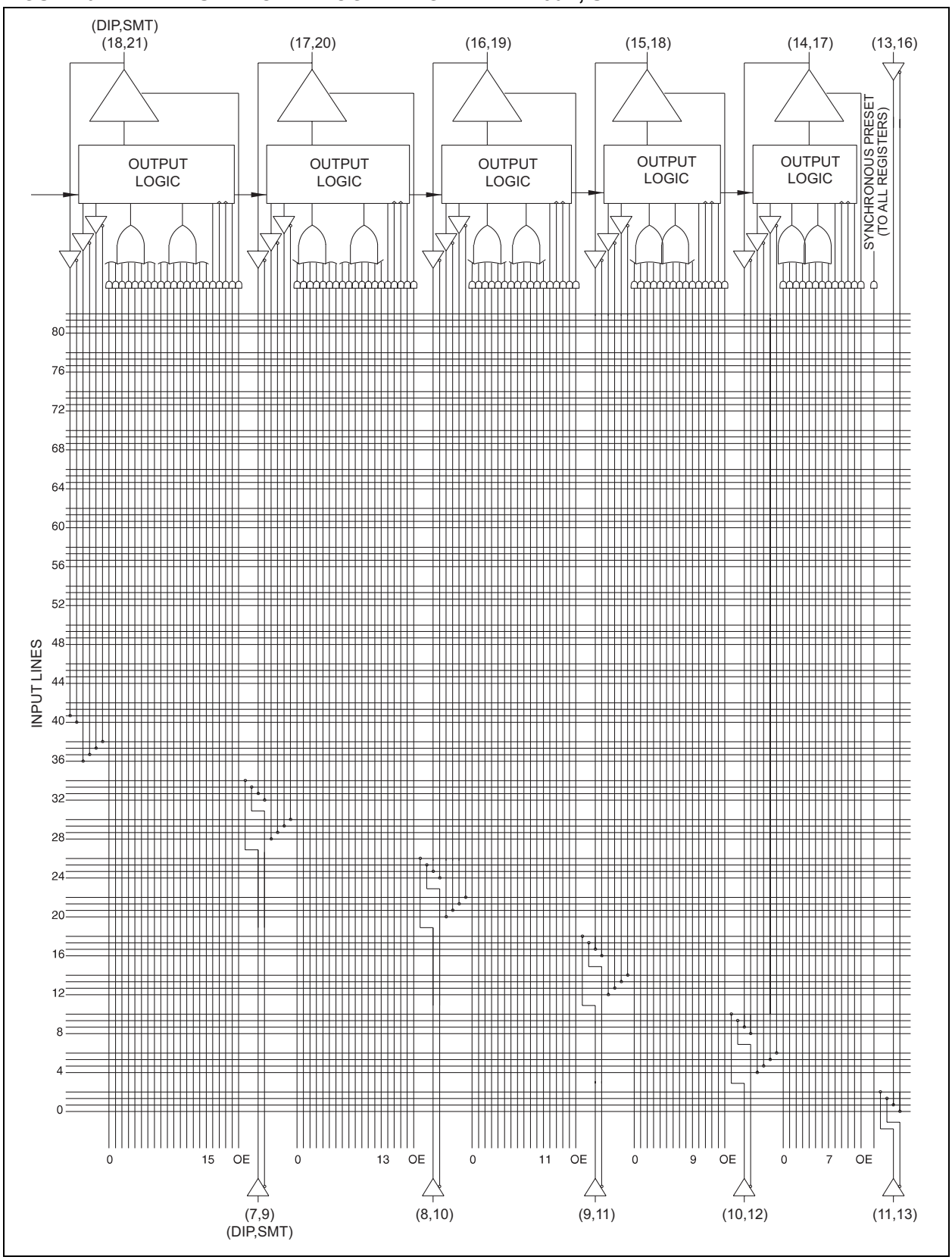
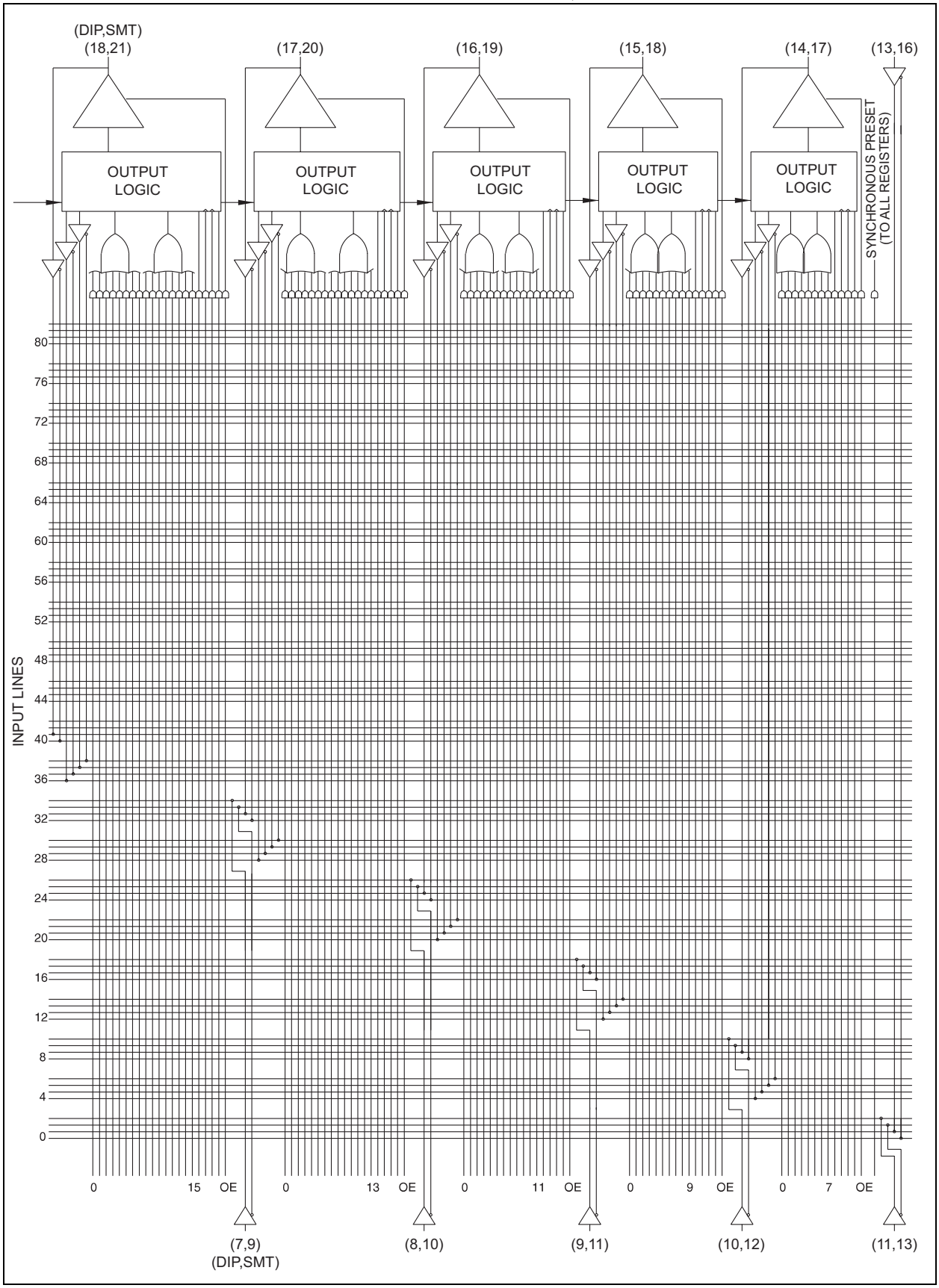


FIGURE 6-2: FUNCTIONAL LOGIC DIAGRAM ATF750C, LOWER HALF



7.0 DEVICE CHARACTERISTICS

FIGURE 7-1: SUPPLY CURRENT VS. SUPPLY VOLTAGE – ATF750C (T_A = 25°C)

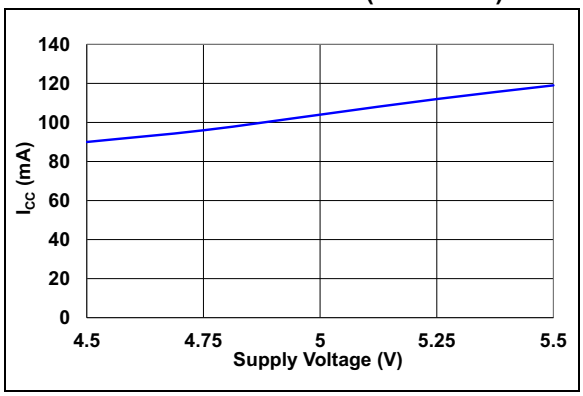


FIGURE 7-2: SUPPLY CURRENT VS. FREQUENCY – ATF750C (T_A = 25°C)

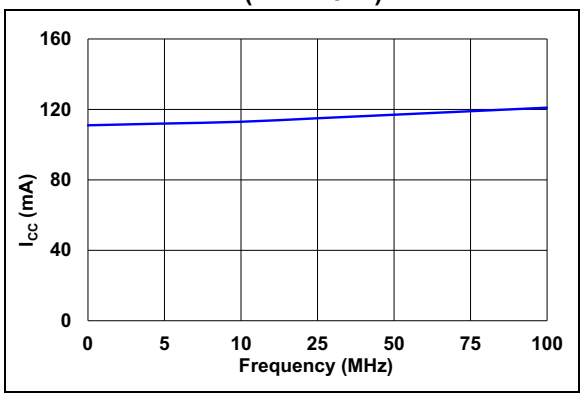


FIGURE 7-3: OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V)

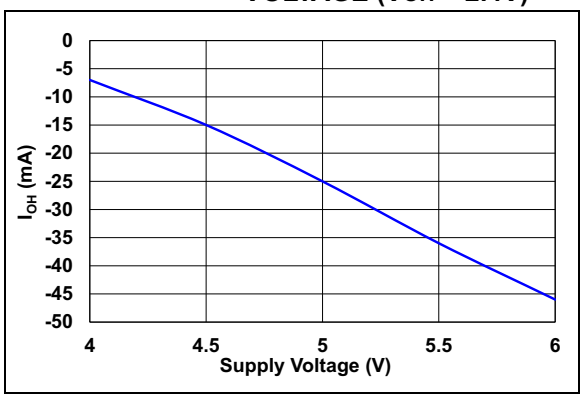


FIGURE 7-4: SUPPLY CURRENT VS. SUPPLY VOLTAGE – ATF750CL (T_A = 25°C)

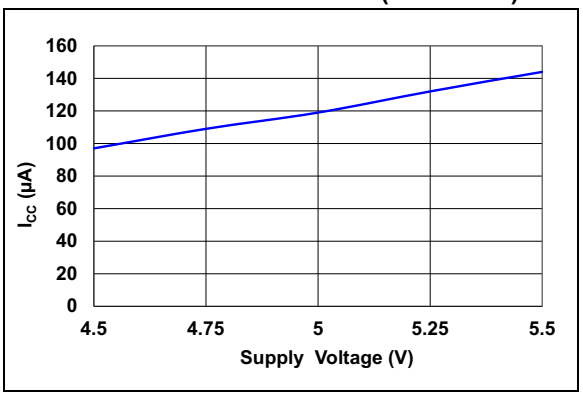


FIGURE 7-5: SUPPLY CURRENT VS. FREQUENCY – ATF750CL (T_A = 25°C)

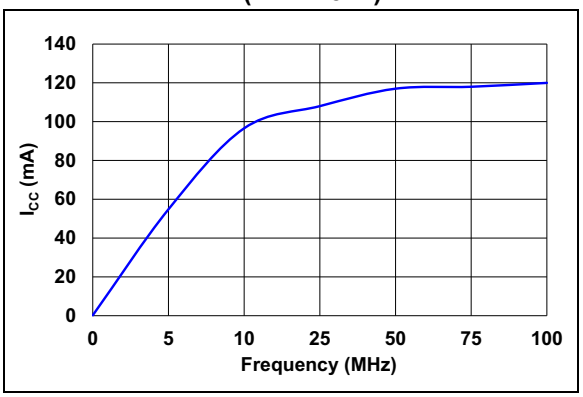


FIGURE 7-6: OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)

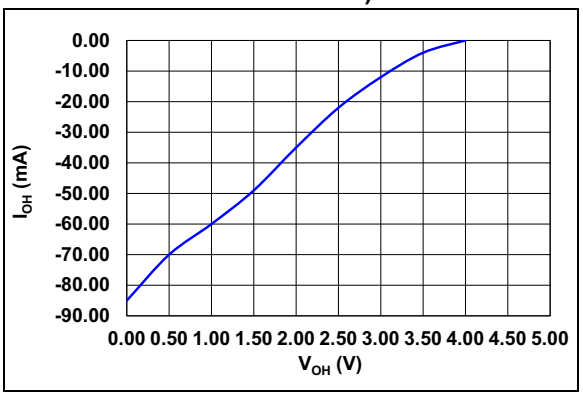


FIGURE 7-7: OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V)

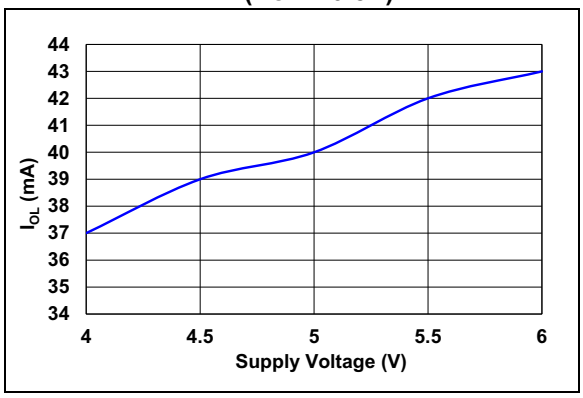


FIGURE 7-8: OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)

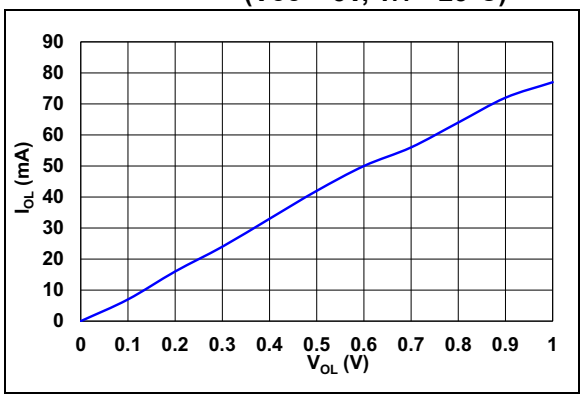


FIGURE 7-9: INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C) WITHOUT PIN-KEEPER

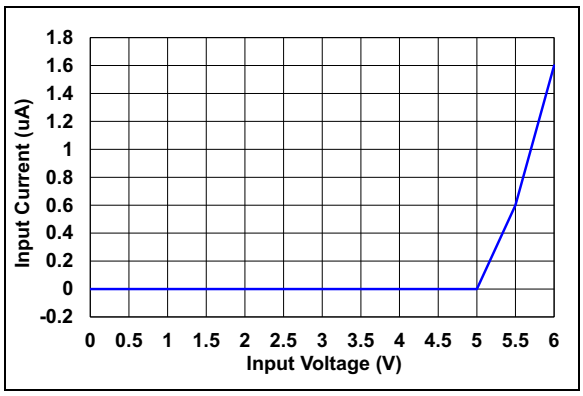


FIGURE 7-10: OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)

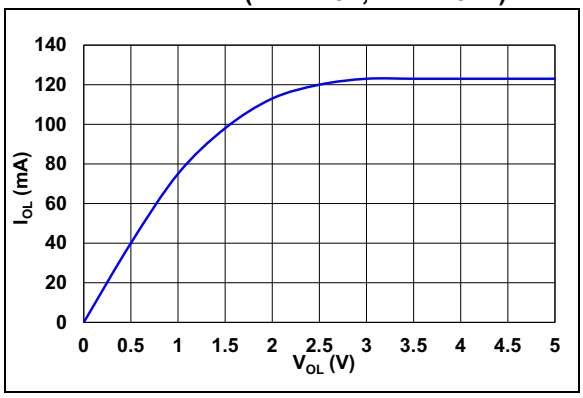


FIGURE 7-11: INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)

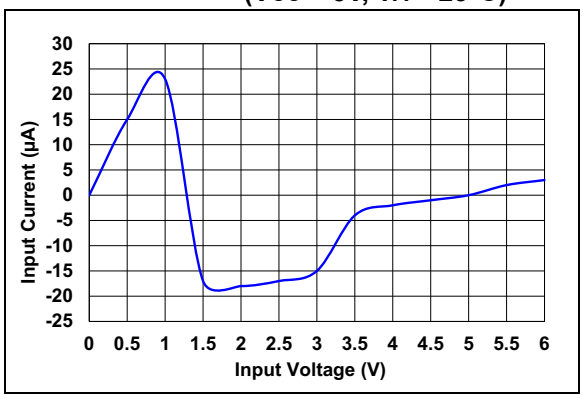
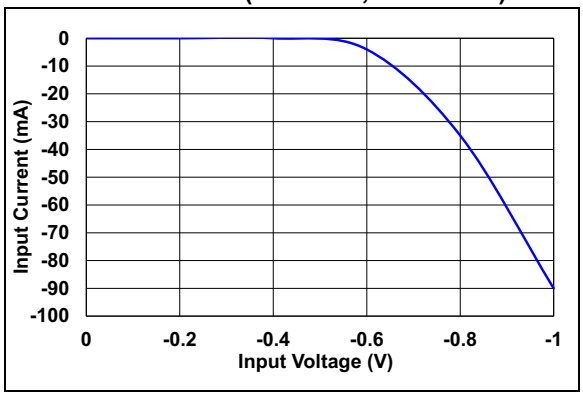


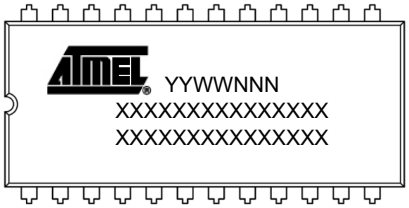
FIGURE 7-12: INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 5V, T_A = 25°C)



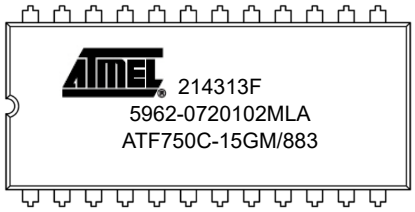
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

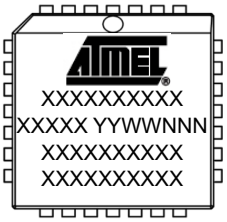
24-Lead CerDIP



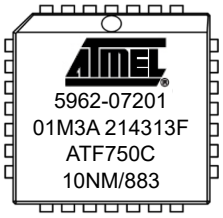
Example



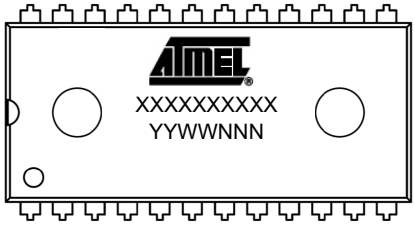
28-Lead CLCC



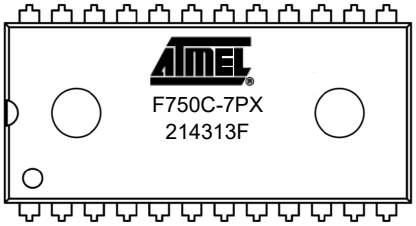
Example



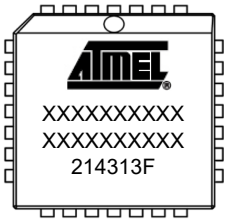
24-Lead PDIP



Example

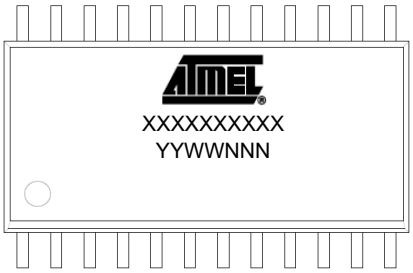


28-Lead PLCC

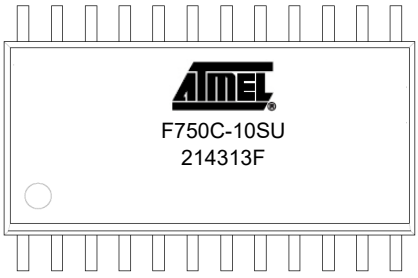


Example

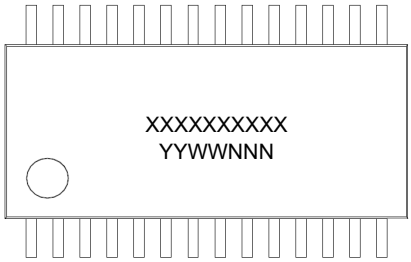
24-Lead SOIC



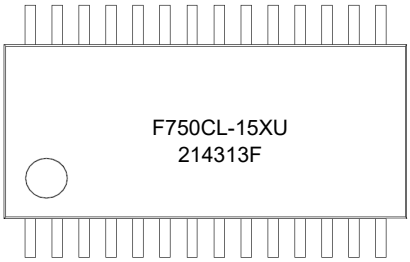
Example



24-Lead TSSOP



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	*	This packages are RoHs compliant. The JEDEC® designator can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

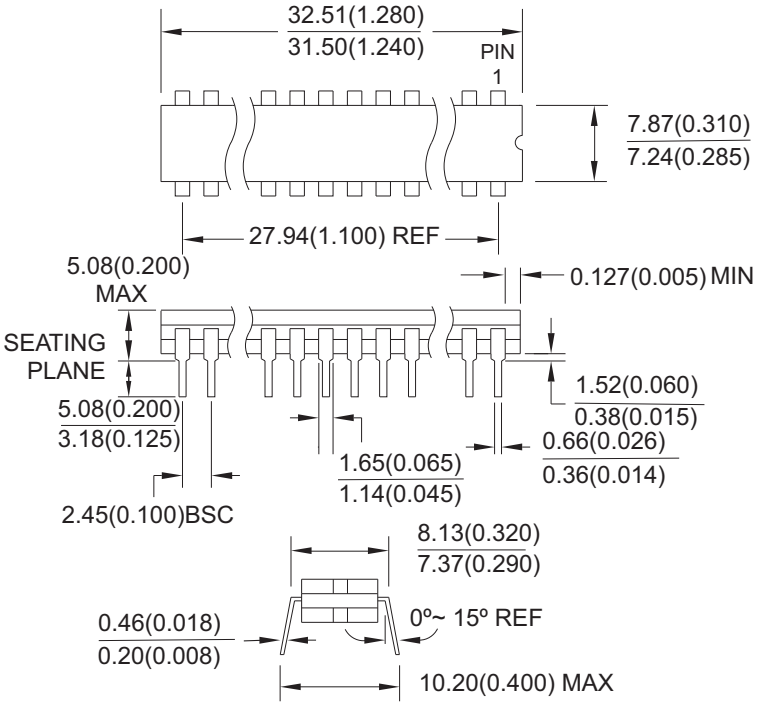
8.2 Thermal Resistance

The following table summarizes the thermal resistance data for the package types available.

TABLE 8-1: THERMAL RESISTANCE DATA

Package Type	θJA	θJC
24-lead CerDIP	65 °C/W	9 °C/W
28-lead CLCC	72 °C/W	16 °C/W
24-lead PDIP	60 °C/W	22 °C/W
28-lead PLCC	38 °C/W	16 °C/W
24-lead SOIC	46 °C/W	17 °C/W
24-lead TSSOP	67 °C/W	60 °C/W

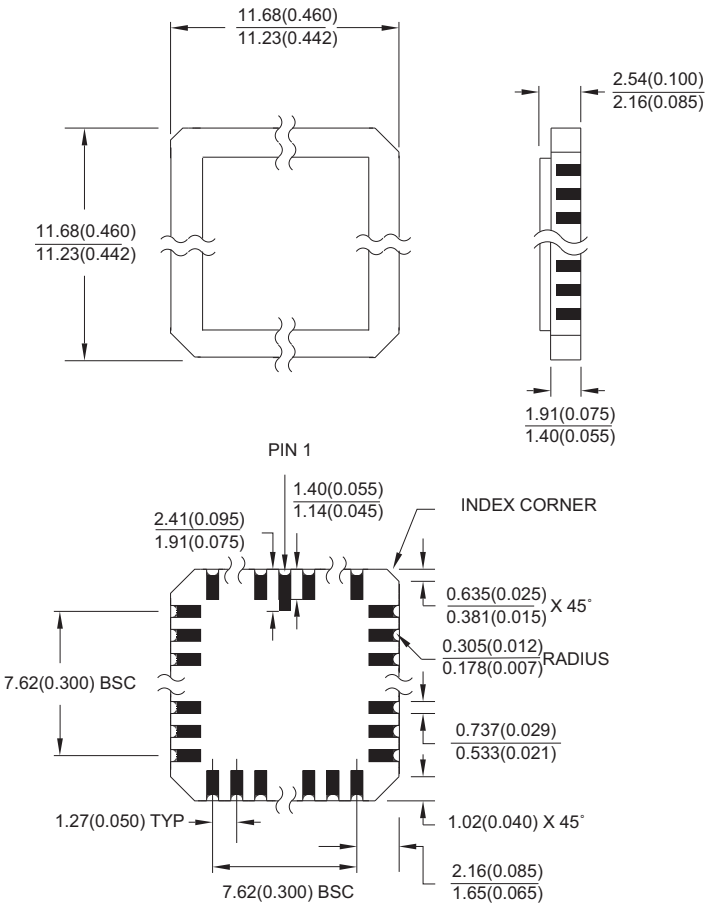
Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 D-9 Config A (Glass Sealed)



10/21/03

	TITLE	DRAWING NO.	REV.
	24D3, 24-lead, 0.300" Wide. Non-windowed, Ceramic Dual Inline Package (Cerdip)	24D3	B

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 C-4

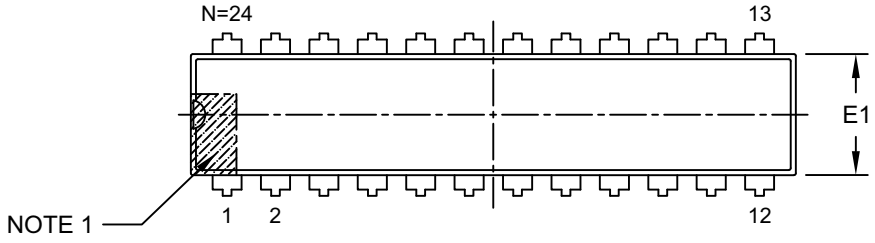


10/21/03

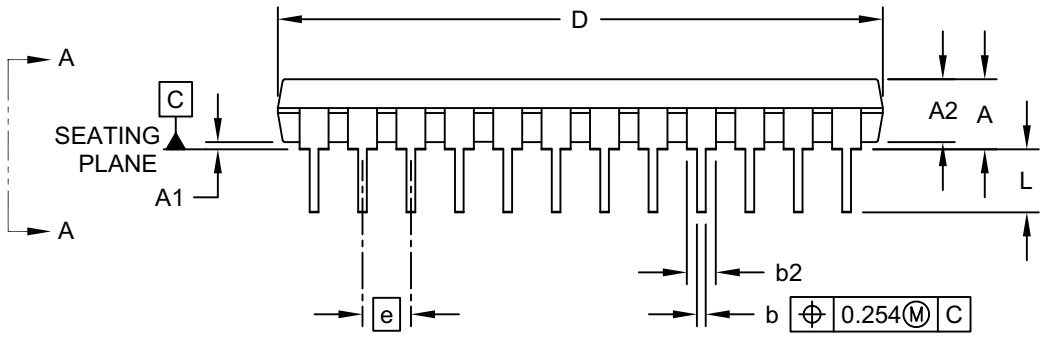
	TITLE	DRAWING NO.	REV.
	28L, 28-pad, Non-windowed, Ceramic Lid, Leadless Chip Carrier (LCC)	28L	B

24-Lead Skinny Plastic Dual In-Line (JDB) - 300 mil Body [SPDIP]
Atmel Legacy Global Pakage Code PHW

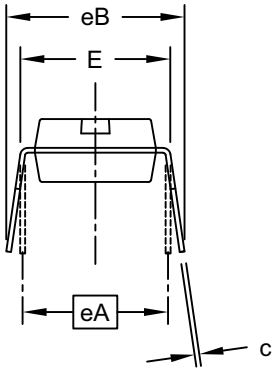
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

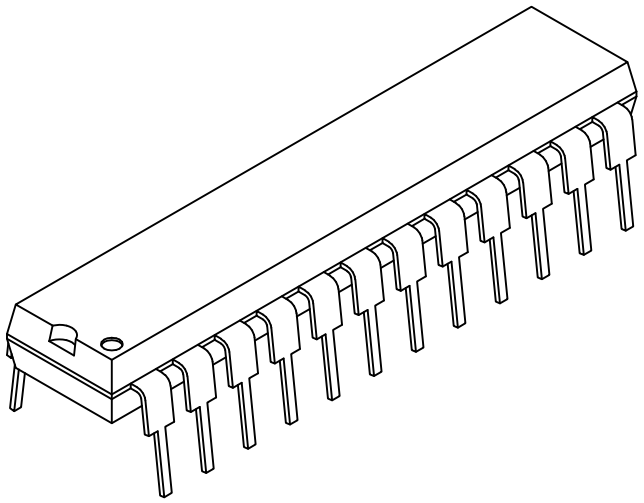


VIEW A-A

Microchip Technology Drawing C04-21286 Rev A Sheet 1 of 2

24-Lead Skinny Plastic Dual In-Line (JDB) - 300 mil Body [SPDIP]
Atmel Legacy Global Pakage Code PHW

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		24	
Pitch	e		2.54 BSC	
Top to Seating Plane	A	-	-	5.334
Molded Package Thickness	A2	2.921	3.302	4.953
Base to Seating Plane	A1	0.381	-	-
Shoulder to Shoulder Width	E	7.620	7.874	8.255
Molded Package Width	E1	6.096	6.350	7.112
Overall Length	D	31.242	31.750	32.512
Tip to Seating Plane	L	2.921	3.302	3.810
Lead Thickness	c	0.203	0.254	0.356
Upper Lead Width	b2	1.143	1.524	1.778
Lower Lead Width	b	0.356	0.457	0.588
Overall Row Spacing	eA		7.62 BSC	
Overall Row Spacing	eB	-	-	10.922

Notes:

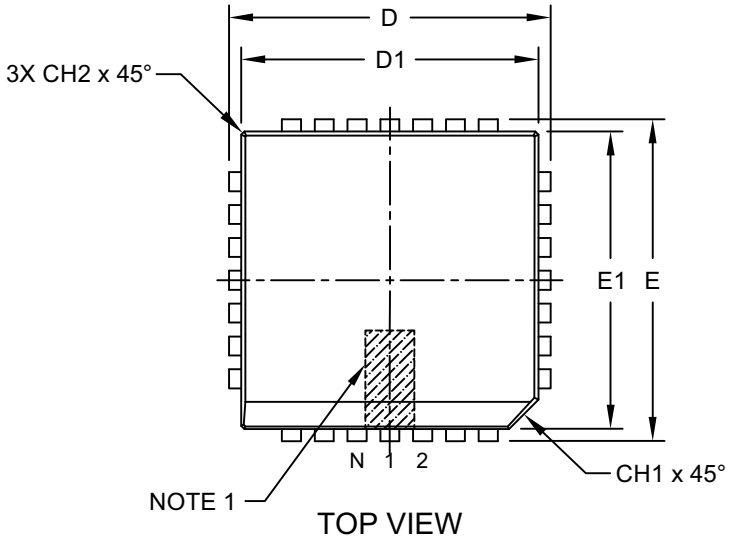
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

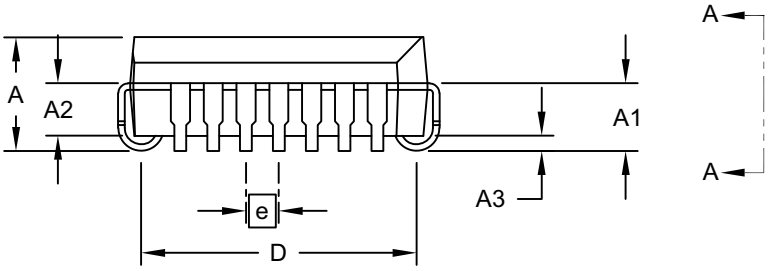
Microchip Technology Drawing C04-21286 Rev A Sheet 2 of 2

28-Lead Plastic Leaded Chip Carrier (LI) - Square [PLCC]

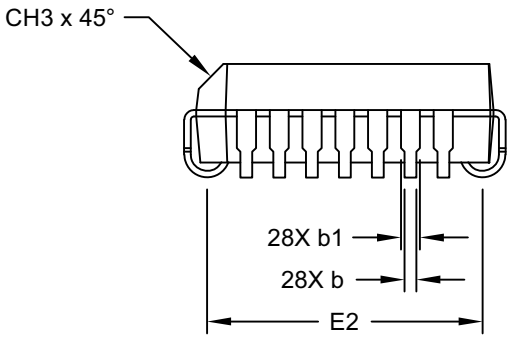
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

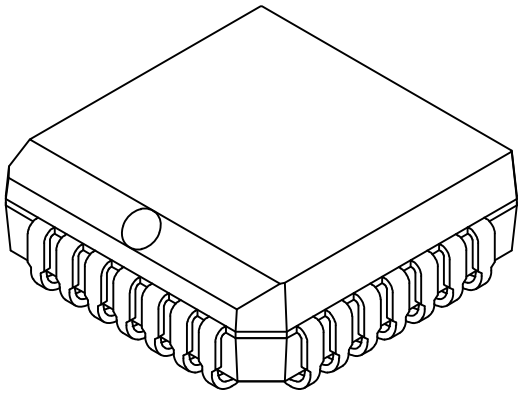


VIEW A-A

Microchip Technology Drawing C04-026-LI Rev C Sheet 1 of 2

28-Lead Plastic Leaded Chip Carrier (LI) - Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	N		28			28	
Pitch	e		.050			1.27	
Overall Height	A	.165	.172	.180	4.19	4.37	4.57
Contact Height	A1	.090	.105	.120	2.29	2.67	3.05
Molded Package to Contact	A2	.062	-	.083	1.57	-	2.11
Standoff §	A3	.020	-	-	0.51	-	-
Corner Chamfer	CH1	.042	-	.048	1.07	-	1.22
Chamfers	CH2	-	-	.020	-	-	0.51
Side Chamfer	CH3	.042	-	.056	1.07	-	1.42
Overall Width	E	.485	.490	.495	12.32	12.45	12.57
Overall Length	D	.485	.490	.495	12.32	12.45	12.57
Molded Package Width	E1	.450	.453	.456	11.43	11.51	11.58
Molded Package Length	D1	.450	.453	.456	11.43	11.51	11.58
Footprint Width	E2	.382	.410	.438	9.70	10.41	11.13
Footprint Length	D2	.382	.410	.438	9.70	10.41	11.13
Lead Thickness	c	.0075	-	.0125	0.19	-	0.32
Upper Lead Width	b1	.025	-	.032	0.64	-	0.81
Lower Lead Width	b	.013	-	.021	0.33	-	0.53

Notes:

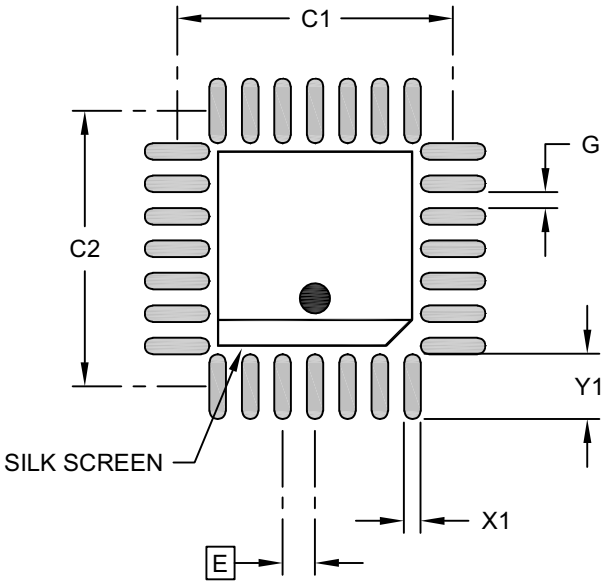
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-026-LI Rev C Sheet 2 of 2

28-Lead Plastic Leaded Chip Carrier (LI) - Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Contact Pitch	E	.050 BSC			1.27 BSC		
Contact Pad Spacing	C1		.425			10.80	
Contact Pad Spacing	C2		.425			10.80	
Contact Pad Width (X28)	X1			.026			0.66
Contact Pad Length (X28)	Y1			.100			2.54
Contact Pad to Center Pad (X24)	G	.008			0.20		

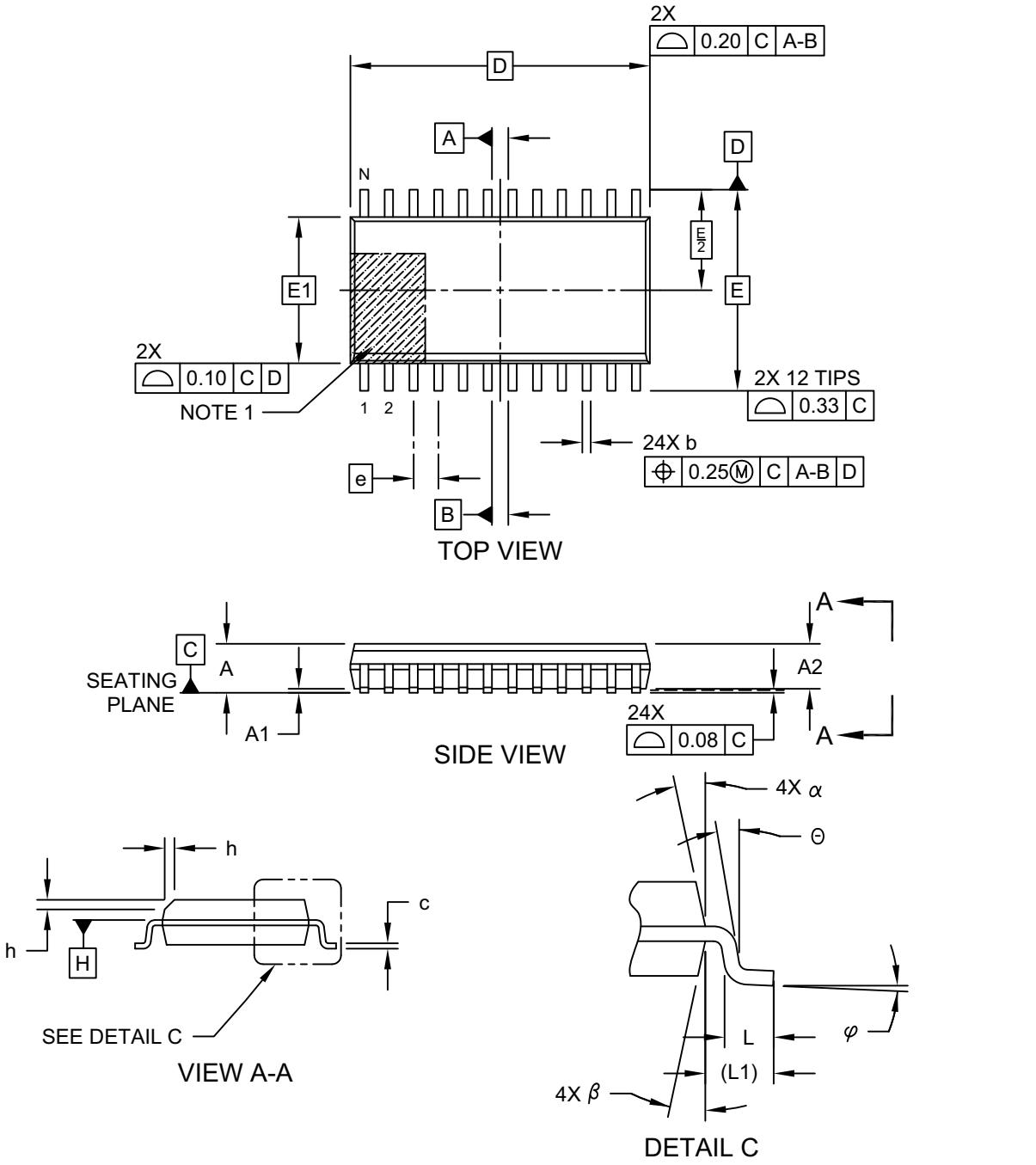
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2026-LI Rev C

24-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

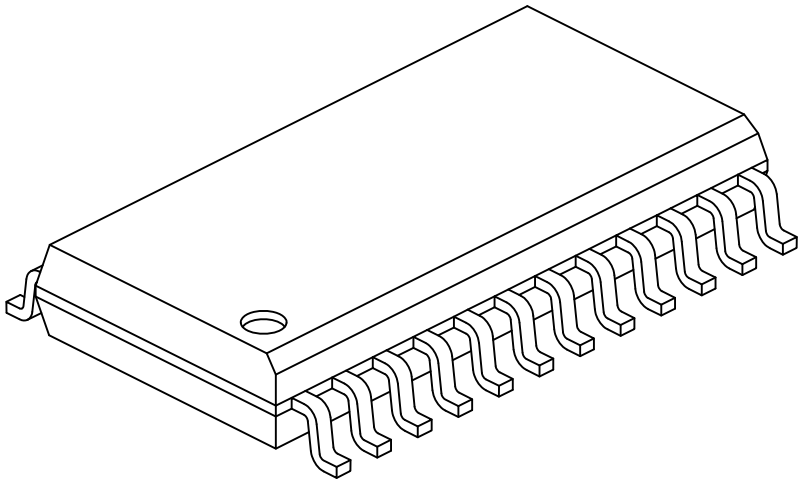
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-025 [SO] Rev E Sheet 1 of 2

24-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		24	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		15.40 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

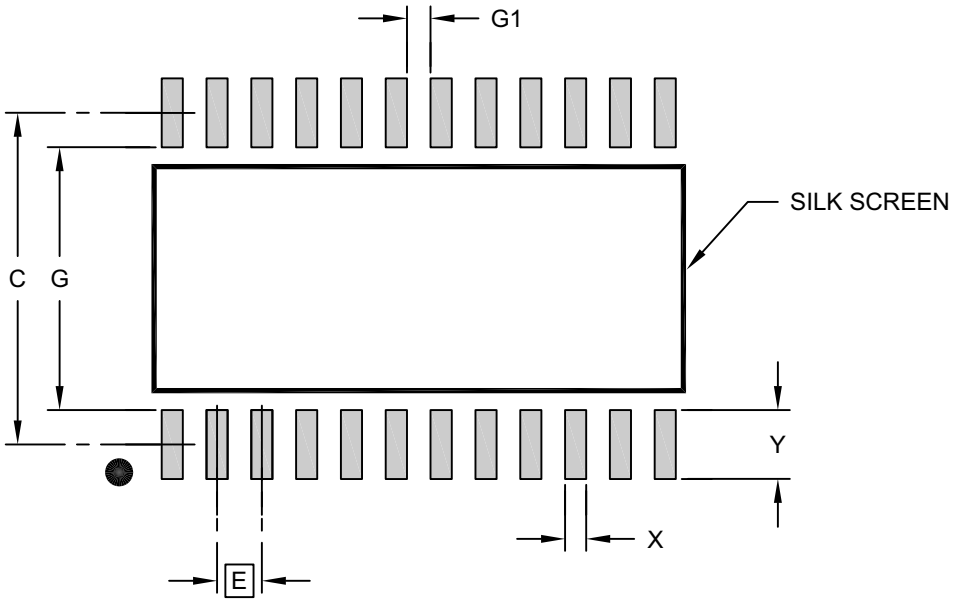
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-025 [SO] Rev E Sheet 2 of 2

24-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.00
Distance Between Pads	G1	0.67		
Distance Between Pads	G	7.40		

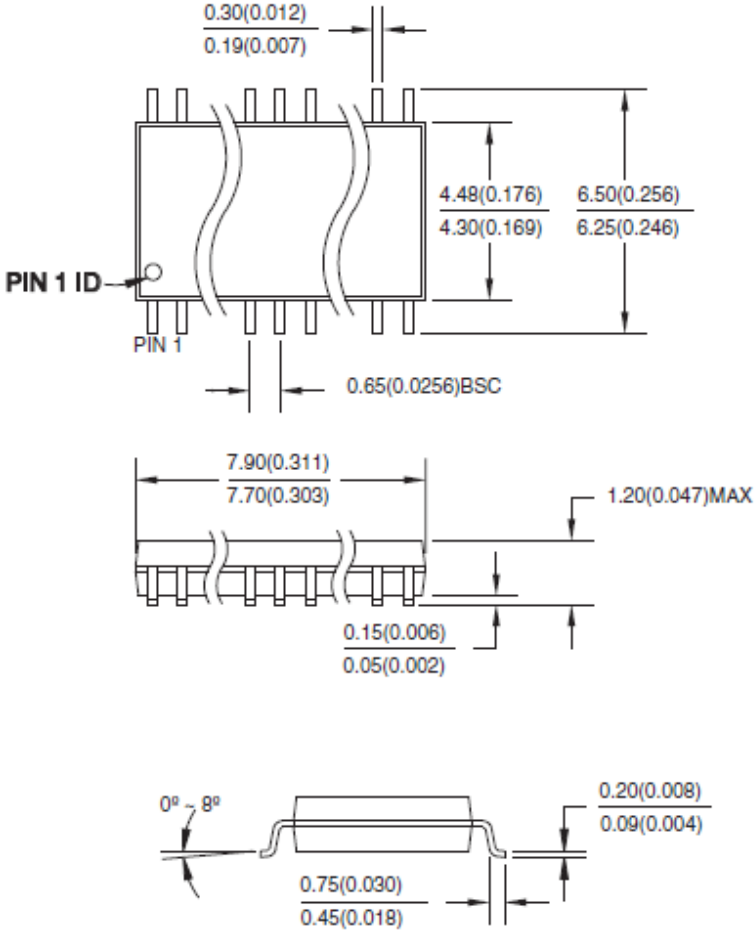
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2025 (SO) Rev B

Dimensions in Millimeter and (Inches)*
JEDEC STANDARD MO-153 AD
Controlling dimension: millimeters



04/11/2001

	TITLE	DRAWING NO.	REV.
	24X, 24-lead (4.4 mm body width) Plastic Thin Shrink Small Outline Package (TSSOP)	24X	A

APPENDIX A: REVISION HISTORY

Revision A (1/2022)

Updated to the Microchip template. Microchip DS20006641 replaces Atmel document 0776.

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PRODUCT IDENTIFICATION SYSTEM

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PART NO.	-XX	X	X	XXX	-[X](1)
Device	Speed Grade	Package Type	Temperature Range	Lead Count	Tape and Reel Option

Device:	ATF750C =	5V Standard-Power CPLD	
	ATF750CL =	5V Low-Power CPLD	
Speed Grade:	7.5 =	7.5 ns (t_{PD})	
	10 =	10 ns (t_{PD})	
	15 =	15 ns (t_{PD})	
Package Type:	G =	CerDIP (Ceramic Dual In-line Package))	
	N =	CLCC (Ceramic Leadless Chip Carrier)	
	S =	SOIC (Plastic Gull Wing Small Outline)	
	X =	TSSOP (Thin Shrink Small Outline)	
	P =	PDIP (Plastic Dual In-line Package)	
	J =	PLCC (Plastic J-leaded Chip Carrier)	
Temperature Range:	U =	-40°C to +85°C (Industrial)	
	X =	0°C to +70°C (Commercial)	
	M =	-55°C to +125°C (Military)	
Lead Count:	24 =	24 Leads	
	28 =	28 Leads	

Examples:

a)	ATF750C-7JX:	Commercial temp., PLCC package.
b)	ATF750C-7PX:	Commercial temp., PDIP package.
c)	ATF750C-7SX:	Commercial temp., SOIC package.
d)	ATF750C-10JU:	Industrial temp., PLCC package.
e)	ATF750C-10PU:	Industrial temp., PDIP package.
f)	ATF750C-10SU:	Industrial temp., SOIC package.
g)	ATF750C-10SU-T:	Industrial temp., Tape and Reel, SOIC package.
h)	ATF750CL-15JU:	Industrial temp., PLCC package.
i)	ATF750CL-15PU:	Industrial temp., PDIP package.
j)	ATF750CL-10SU:	Industrial temp., SOIC package.
k)	ATF750CL-15XU:	Industrial temp., TSSOP package.
l)	ATF750C-10NM/883:	Military temp., CLCC package.
m)	ATF750C-10GM/883:	Military temp., CerDIP package.
n)	ATF750C-15NM/883:	Military temp., CLCC package.
o)	ATF750C-15GM/883:	Military temp., CerDIP package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

ORDERING INFORMATION

ATF750C Military Ordering Information

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAX} (MHz)	Ordering Code	Package	Operation Range
10	7	83	ATF750C-10GM/883	24-Lead CerDIP	Military/883 (-55°C to +125°C) Class B, Fully Compliant
			ATF750C-10NM/883	28-Lead CLCC	
			5962-0720101MLA	24-Lead CerDIP	
			5962-0720101M3A	28-Lead CLCC	
15	10	55	ATF750C-15GM/883	24-Lead CerDIP	
			ATF750C-15NM/883	28-Lead CLCC	
			5962-0720102MLA	24-Lead CerDIP	
			5962-0720102M3A	28-Lead CLCC	

ATF750C(L) Green Package Options (Pb/Halide-Free/RoHS Compliant)

t_{PD} (ns)	t_{COS} (ns)	Ext. f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	6.5	95	ATF750C-7JX	28-Lead PLCC	Commercial (0°C to +70°C)
			ATF750C-7PX	24-Lead PDIP	
			ATF750C-7SX	24-Lead SOIC	
10	7	83	ATF750C-10JU	28-Lead PLCC	Industrial (-40°C to +85°C)
			ATF750C-10PU	24-Lead PDIP	
			ATF750C-10SU	24-Lead SOIC	
15	10	44	ATF750CL-15JU	28-Lead PLCC	Industrial (-40°C to +85°C)
			ATF750CL-15PU	24-Lead PDIP	
			ATF750CL-15SU	24-Lead SOIC	
			ATF750CL-15XU	24-Lead TSSOP	

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