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CYPRESS
EMBEDDED IN TOMORROW™

CY62157G/CY62157GE MoBL

8-Mbit (512K × 16-bits) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby current
  - Typical standby current: 1.4 µA
  - Maximum standby current: 6.5 µA
- High speed: 45 ns
- Voltage range: 1.65 V to 3.6 V
- Embedded Error-Correcting Code (ECC) for single-bit error correction
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA, 44-TSOP II and 48-pin TSOP I packages

Functional Description

CY62157G and CY62157GE are high-performance CMOS low-power (MoBL®) SRAM device with Embedded Error-Correcting Code. ECC logic can detect and correct single bit error in accessed location.

This device is offered in dual chip enable option. Dual chip enable devices are accessed by asserting both chip enable inputs – $\overline{CE}_1$ as LOW and CE_2 as HIGH.

Data writes are performed by asserting the Write Enable input ($\overline{WE}$ LOW), and providing the data and address on device data (I/O_0 through I/O_{15}) and address (A_0 through A_{18}) pins respectively. The Byte High/Low Enable ($\overline{BHE}$, $\overline{BLE}$) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). Byte accesses can be performed by asserting the required byte enable signal ($\overline{BHE}$, $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH/CE_2 LOW for dual chip enable device), or control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

These devices also have a unique “Byte Power down” feature, where, if both the Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) are disabled, the devices seamlessly switch to standby mode irrespective of the state of the chip enable(s), thereby saving power.

The CY62157G and CY62157GE devices are available in a Pb-free 48-ball VFBGA, 44-TSOP II and 48-pin TSOP I packages. See the Logic Block Diagram – CY62157G on page 2.

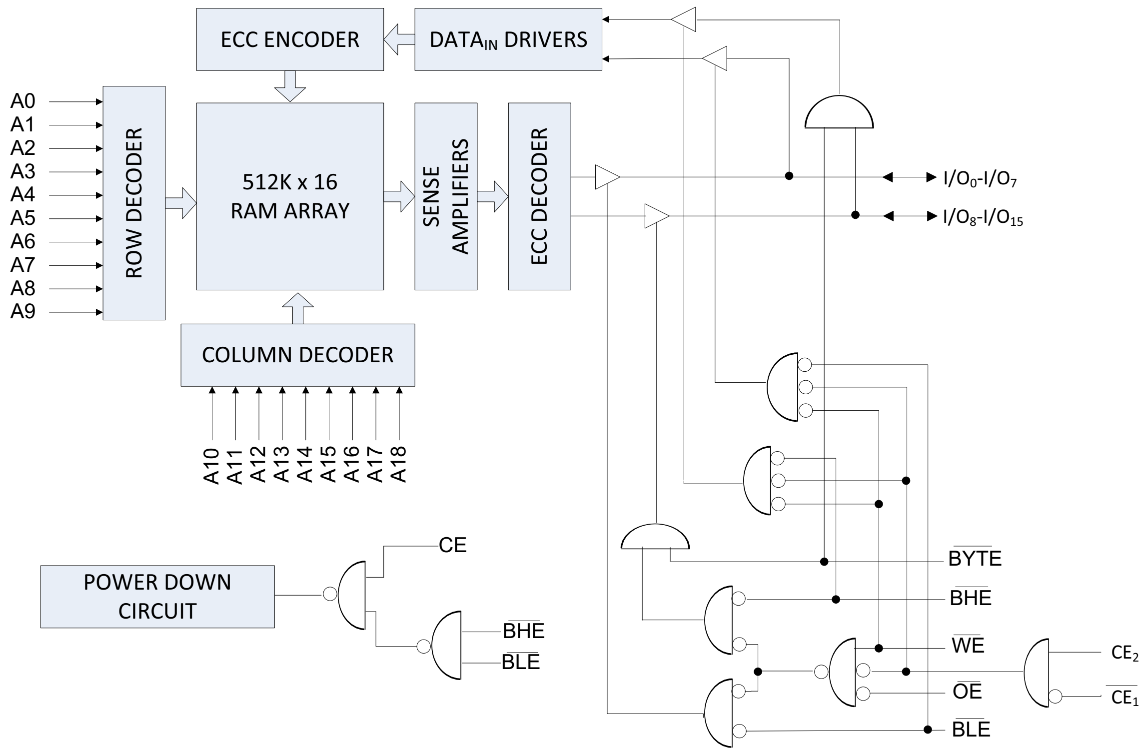
The device in the 48-pin TSOP I package can also be configured to function as a 1M × 8-bit device. See the Pin Configurations on page 5.

Product Portfolio

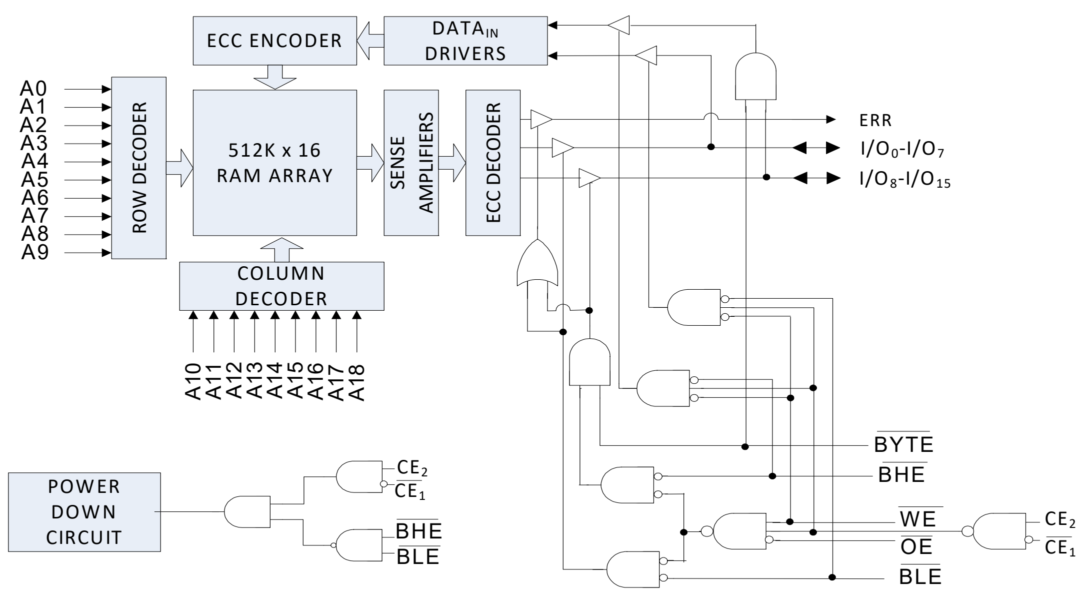
Product	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
				Operating I_{CC}, (mA) $f = f_{max}$		Standby, I_{SB2} (µA)	
				Typ[1]	Max	Typ[1]	Max
CY62157G18	Industrial	1.65 V–2.2 V	55	18	22	2.0	8
CY62157G30	Industrial	2.2 V–3.6 V	45	18	25	1.4	6.5

Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V) and V_{CC} = 1.8V (for V_{CC} range of 1.65 V–2.2 V), T_A = 25 °C.

Logic Block Diagram – CY62157G



Logic Block Diagram – CY62157GE



Contents

Pin Configurations

Figure 1. 48-ball VFBGA Pinout (Top View)[2]

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	CE_2
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}_1$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

Figure 2. 48-ball VFBGA Pinout (with ERR (Top View))[2]

	1	2	3	4	5	6
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	CE_2
B	I/O_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}_1$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	ERR	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

Figure 3. 44-pin TSOP II Pinout (Top View)[2]

A_4	1	44	A_5
A_3	2	43	A_6
A_2	3	42	A_7
A_1	4	41	$\overline{OE}$
A_0	5	40	$\overline{BHE}$
$\overline{CE}$	6	39	$\overline{BLE}$
I/O_0	7	38	I/O_{15}
I/O_1	8	37	I/O_{14}
I/O_2	9	36	I/O_{13}
I/O_3	10	35	I/O_{12}
V_{CC}	11	34	V_{SS}
V_{SS}	12	33	V_{CC}
I/O_4	13	32	I/O_{11}
I/O_5	14	31	I/O_{10}
I/O_6	15	30	I/O_9
I/O_7	16	29	I/O_8
$\overline{WE}$	17	28	A_8
A_{18}	18	27	A_9
A_{17}	19	26	A_{10}
A_{16}	20	25	A_{11}
A_{15}	21	24	A_{12}
A_{14}	22	23	A_{13}

Note

2. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configurations (continued)

Figure 4. 48-pin TSOP I Pinout (Top View)[3, 4]

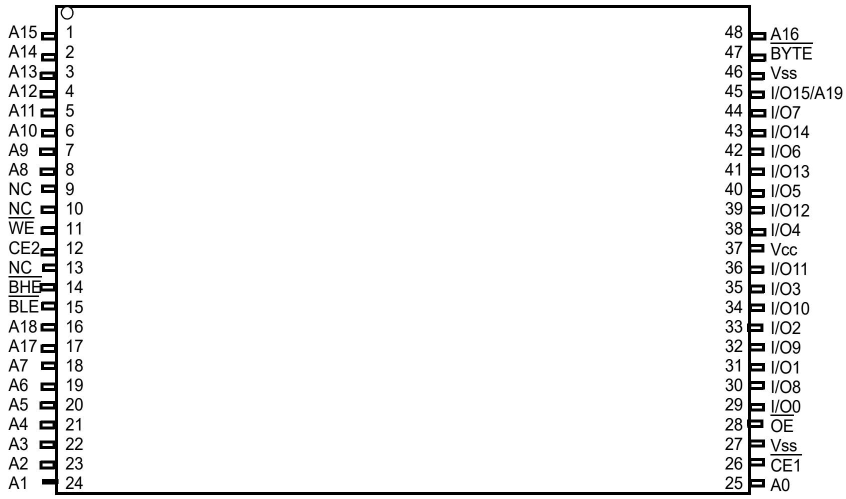
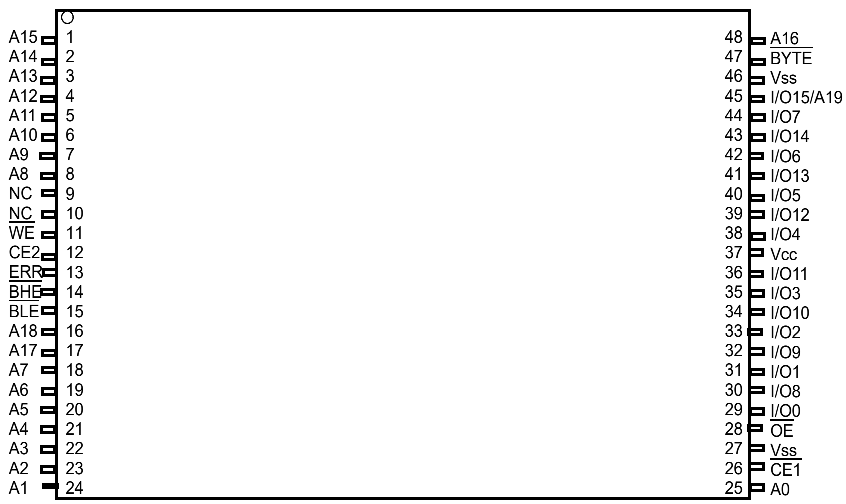


Figure 5. 48-pin TSOP I Pinout (with ERR (Top View))[3, 4]



Notes

3. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
4. Tie the $\overline{BYTE}$ pin in the 48-pin TSOP I package to V_{CC} to use the device as a 512K × 16 SRAM. The 48-pin TSOP I package can also be used as a 1M × 8 SRAM by tying the $\overline{BYTE}$ signal to V_{SS}. In the 1M × 8 configuration, Pin 45 is the extra address line A19, while $\overline{BHE}$, $\overline{BLE}$, and I/O_8 to I/O_{14} pins are not used and can be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to + 150 °C

Ambient temperature with power applied .... –55 °C to + 125 °C

Supply voltage to ground potential .... –0.2 V to V_{CC} + 0.3 V

DC voltage applied to outputs in High Z state[5] .... –0.2 V to V_{CC} + 0.3 V

DC input voltage[5] .... –0.2 V to V_{CC} + 0.3 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage (HBM) (MIL-STD-883, Method 3015) .... >2001 V

Latch-up current .... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V 2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter	Description		Test Conditions		45/55 ns Min	45/55 ns Typ[6]	45/55 ns Max	Unit
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA		2	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2	V
		2.2 V to 2.7 V	–		1.8	–	V_{CC} + 0.3	
		2.7 V to 3.6 V	–		2	–	V_{CC} + 0.3	
V_{IL}	Input LOW voltage[6]	1.65 V to 2.2 V	–		–0.2	–	0.4	V
		2.2 V to 2.7 V	–		–0.3	–	0.6	
		2.7 V to 3.6 V	–		–0.3	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1	–	+1	
I_{CC}	V_{CC} operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	–	18	25	mA
				f = 18.18 MHz (55 ns)	–	18	22	
				f = 1 MHz	–	6	7	
I_{SB1}[7]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V		$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V, ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = $V_{CC(max)}$		–	1.4	6.5	µA
	Automatic power down current – CMOS inputs; V_{CC} = 1.65 to 2.2 V				–	2.0	8.0	

Notes

5. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V) and V_{CC} = 1.8V (for V_{CC} range of 1.65 V–2.2 V), T_A = 25 °C.
7. Chip enables ($\overline{CE_1}$ and CE_2) must be tied to CMOS levels to meet the I_{SB1}/I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.
8. The I_{SB2} limits at 25 °C, 40 °C, 70 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

DC Electrical Characteristics (continued)

Over the Operating Range of –40 °C to 85 °C

Parameter	Description	Test Conditions		45/55 ns Min	45/55 ns Typ[6]	45/55 ns Max	Unit
I_{SB2}[7]	Automatic power down current – CMOS inputs V_{CC} = 2.2 to 3.6 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$	25 °C[8]	–	1.4	2.8	µA
			40 °C[8]	–	–	3.5	
			70 °C[8]	–	–	5.5	
			85 °C	–	–	6.5	
	Automatic power down current – CMOS inputs V_{CC} = 1.65 to 2.2 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = V_{CC(max)}$		–	2.0	8.0	µA

Notes
5. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V) and V_{CC} = 1.8V (for V_{CC} range of 1.65 V–2.2 V), T_A = 25 °C.
7. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
8. The I_{SB2} limits at 25 °C, 40 °C, 70 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

Parameter[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	

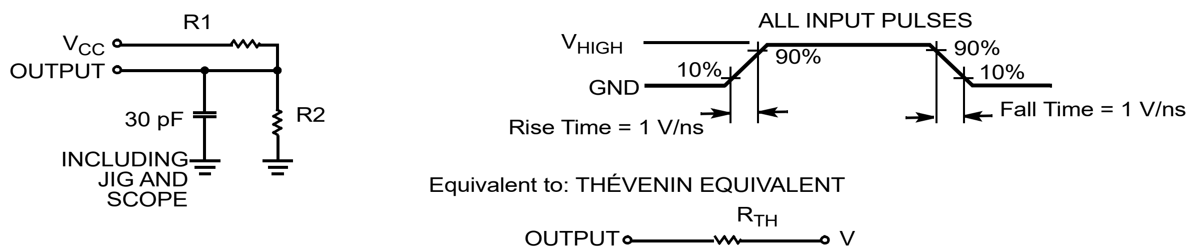
Thermal Resistance

Parameter[9]	Description	Test Conditions	48-pin TSOP I	48-ball VFBGA	44-TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	60.07	36.92	65.91	°C/W
Θ_{JC}	Thermal resistance (junction to case)		9.73	13.55	13.96	

Note
9. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 6. AC Test Loads and Waveforms



Parameters	1.8 V	2.5 V	3.0 V	Unit
R1	13500	16667	1103	Ω
R2	10800	15385	1554	
R_{TH}	6000	8000	645	
V_{TH}	0.8	1.20	1.75	V

Data Retention Characteristics

Over the Operating Range

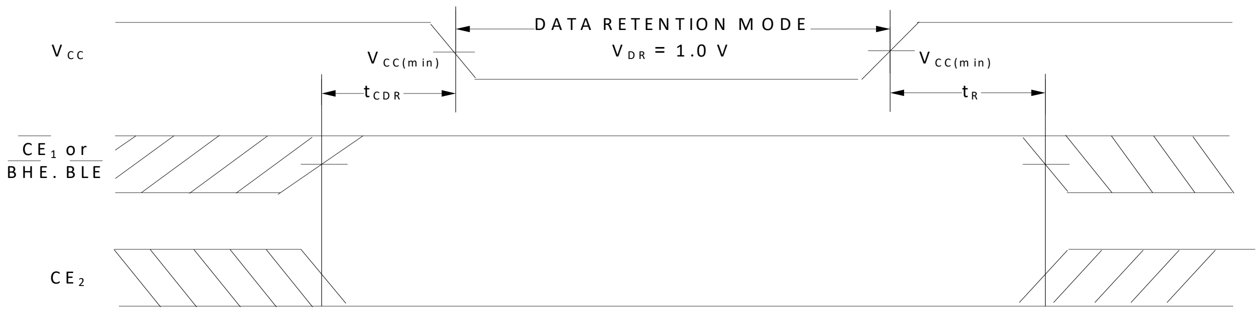
Parameter	Description	Conditions		Min	Typ[15]	Max	Unit
V_{DR}	V_{CC} for data retention			1	–	–	V
I_{CCDR}[11, 12]	Data retention current (For 3.3V Typical Device)	$\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	V_{CC} = 1.2 V	–	4.0	9.0	µA
		$\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	V_{CC} = 1.5 V	–	3.2	8.0	
		$\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	2.2 V < $V_{CC} \leq$ 3.6 V	–	1.4	6.5	
I_{CCDR}[11, 12]	Data retention current (For 1.8V Typical Device)	1.2 V < $V_{CC} \leq$ 2.2 V, $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V		–	5.0	9.0	
t_{CDR}[13]	Chip deselect to data retention time	–		0	–	–	–
t_R[14]	Operation recovery time	–		45/55	–	–	ns

Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.
11. Chip enables ($\overline{CE_1}$ and CE_2) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
12. I_{CCDR} is guaranteed only after the device is firs powered up to V_{CC}(min) and then brought down to V_{DR}.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.

Data Retention Waveform

Figure 7. Data Retention Waveform[15]



Note

15. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Parameter[16]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	
t_{AA}	Address to data valid/Address LOW to ERR valid	–	45	–	55	
t_{OHA}	Data hold from address change	10	–	10	–	
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid/$\overline{CE}$ LOW to ERR valid	–	45	–	55	
t_{DOE}	$\overline{OE}$ LOW to data valid/$\overline{OE}$ LOW to ERR valid	–	22	–	25	
t_{LZOE}	$\overline{OE}$ LOW to Low Z[17]	5	–	5	–	
t_{HZOE}	$\overline{OE}$ HIGH to High Z[17, 18]	–	18	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low-Z[17]	10	–	10	–	
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High-Z[17, 18]	–	18	–	18	
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	0	–	
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	45	–	55	
t_{DBE}	BLE / BHE LOW to data valid	–	45	–	55	
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z[17]	5	–	5	–	
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z[17, 18]	–	18	–	18	
Write Cycle[19, 20]						
t_{WC}	Write cycle time	45	–	55	–	
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	40	–	
t_{AW}	Address setup to write end	35	–	40	–	
t_{HA}	Address hold from write end	0	–	0	–	
t_{SA}	Address setup to write start	0	–	0	–	
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	40	–	
t_{SD}	Data setup to write end	25	–	25	–	
t_{HD}	Data hold from write end	0	–	0	–	
t_{HZWE}	$\overline{WE}$ LOW to High-Z[17, 18]	–	18	–	20	
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[17]	10	–	10	–	

Notes

16. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
20. The minimum write cycle pulse width for Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 8. Read Cycle No. 1 of CY62157G (Address Transition Controlled)[21, 22]

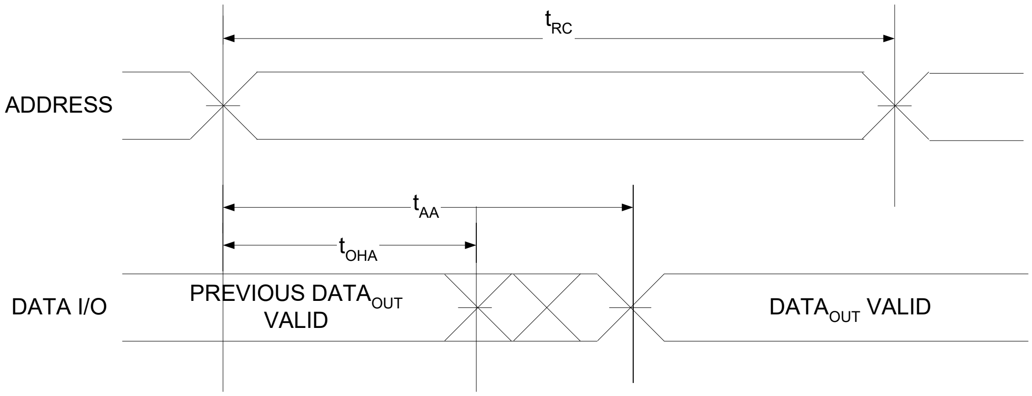
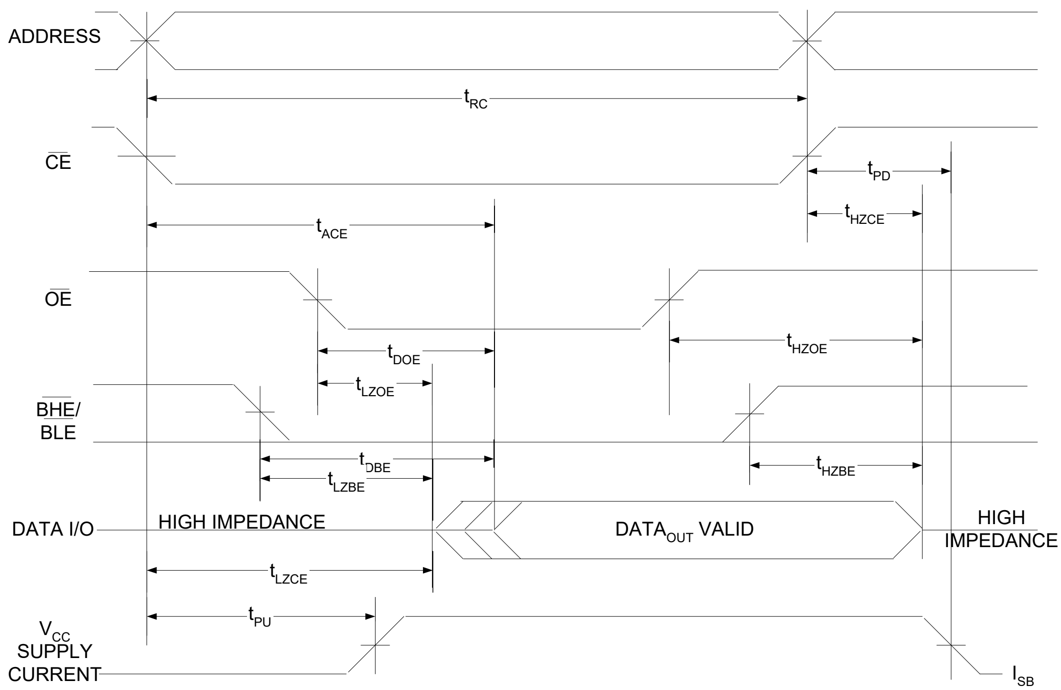


Figure 9. Read Cycle No. 2 ($\overline{OE}$ Controlled)[22, 23, 24]

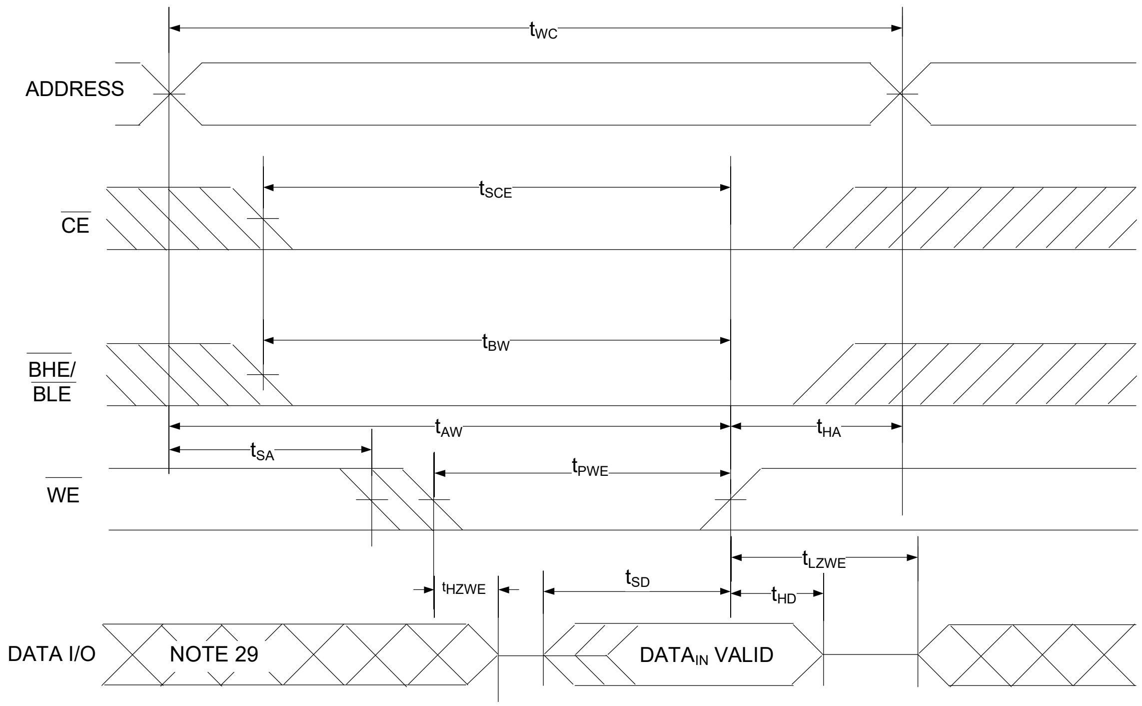


Notes

21. The device is continuously selected. $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
22. $\overline{WE}$ is HIGH for read cycle.
23. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
24. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[25, 26, 27, 28]

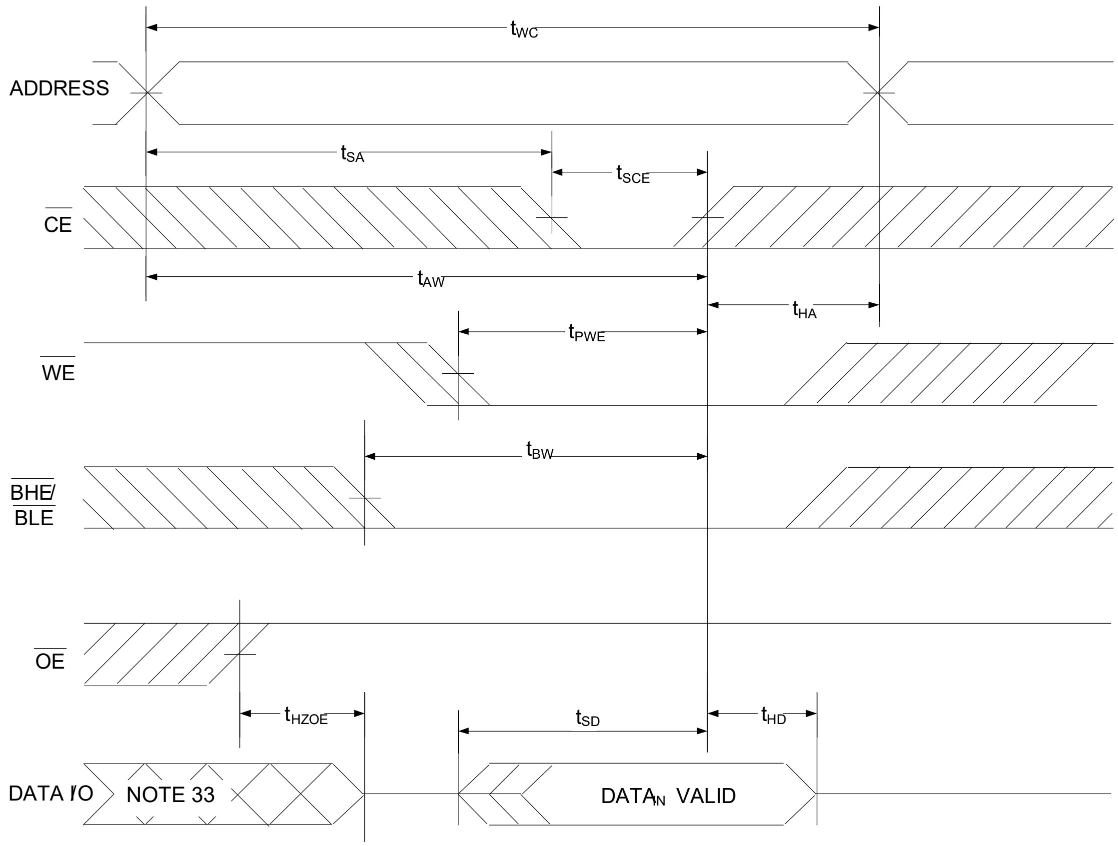


Notes

25. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
26. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both $= V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
27. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
28. The minimum write cycle pulse width for Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD}.
29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 11. Write Cycle No. 2 ($\overline{CE}$ Controlled)[30, 31, 32]

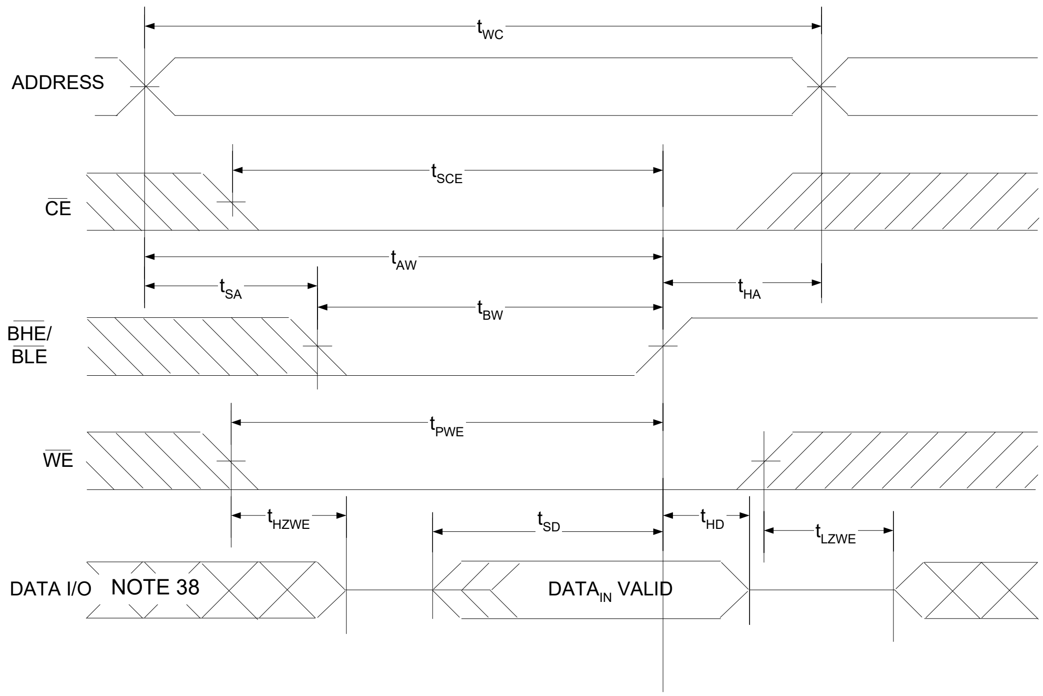


Notes

30. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
31. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
32. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
33. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 12. Write Cycle No. 3 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[34, 35, 36, 37]

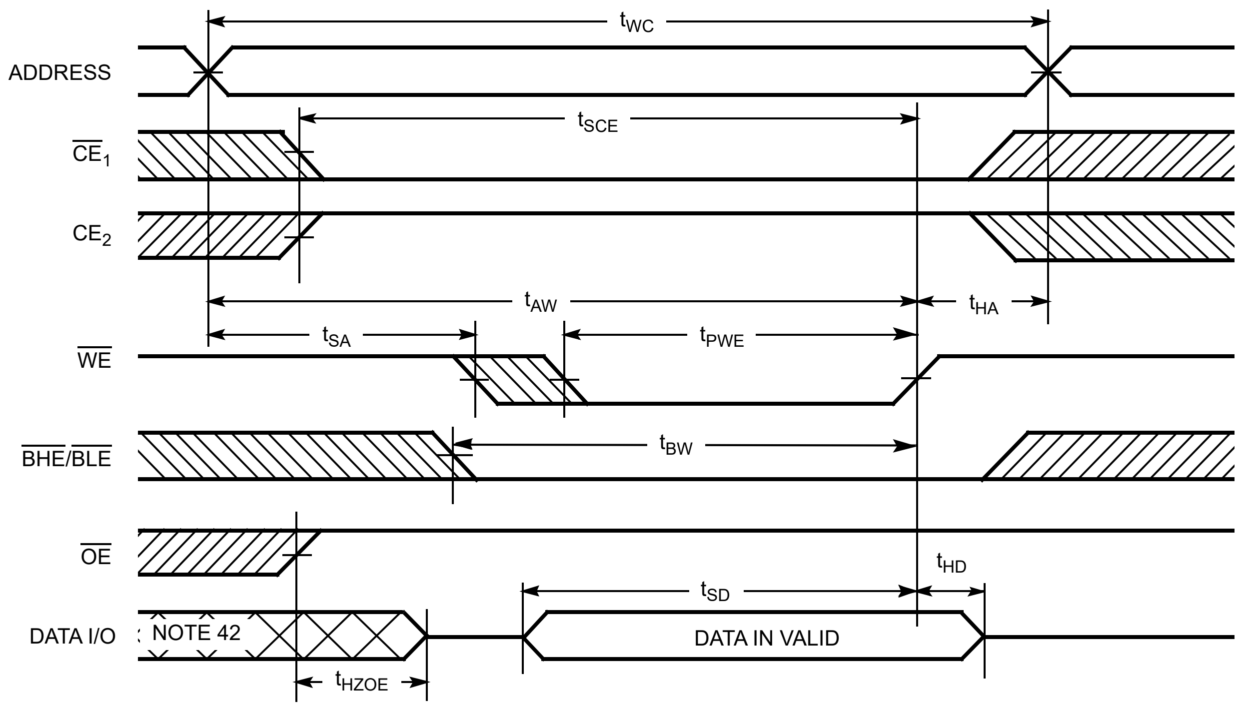


Notes

34. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
35. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
36. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.
37. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD}.
38. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 13. Write Cycle No. 4 ($\overline{WE}$ Controlled)[39, 40, 41]



Notes

39. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
40. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
41. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
42. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table – CY62157G/CY62157GE

BYTE [43]	$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power	Configuration
X[44]	H	X[44]	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})	1M × 8/512K× 16
X	X[44]	L	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})	1M × 8/512K× 16
X	X[44]	X[44]	X	X	H	H	High-Z	Deselect/Power-down	Standby (I_{SB})	512K × 16
H	L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})	512K × 16
H	L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})	512K × 16
H	L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})	512K × 16
H	L	H	H	H	L	H	High-Z	Output disabled	Active (I_{CC})	512K × 16
H	L	H	H	H	H	L	High-Z	Output disabled	Active (I_{CC})	512K × 16
H	L	H	H	H	L	L	High-Z	Output disabled	Active (I_{CC})	512K × 16
H	L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})	512K × 16
H	L	H	L	X	H	L	Data In (I/O_0–I/O_7); High-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})	512K × 16
H	L	H	L	X	L	H	High-Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})	512K × 16
L	L	H	H	L	X	X	Data Out (I/O_0–I/O_7)	Read	Active (I_{CC})	1M × 8
L	L	H	H	H	X	X	High-Z	Output disabled	Active (I_{CC})	1M × 8
L	L	H	L	X	X	X	Data In (I/O_0–I/O_7)	Write	Active (I_{CC})	1M × 8

ERR Output – CY62157GE

Output[45]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected / outputs disabled / Write operation

Notes

43. This pin is available only in the 48-pin TSOP I package. Tie the $\overline{BYTE}$ to V_{CC} to configure the device in the 512K × 16 option. The 48-pin TSOP I package can also be used as a 1M × 8 SRAM by tying the BYTE signal to V_{SS}.
44. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.
45. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157G30-45BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	Industrial
	CY62157G30-45BVXIT			
	CY62157GE30-45BVXI			
	CY62157G30-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	
	CY62157G30-45ZXI	51-85183	48-pin TSOP I (12 × 18.4 × 1.0 mm) (Pb-free)	
	CY62157GE30-45ZXI			
55	CY62157G18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48	
	CY62157G18-55BVXIT			

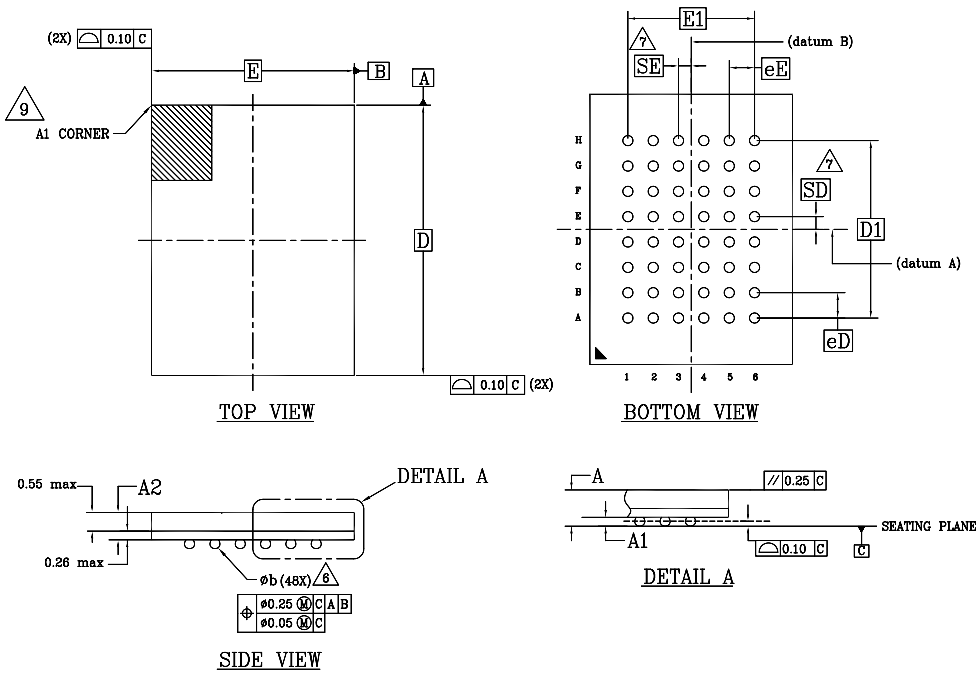
Ordering Code Definitions

CY 621 5 7 G E XX - XX XX X I X

- X = blank or T
  blank = Bulk; T = Tape and Reel
- Temperature Grade:
  I = Industrial
- Pb-free
- Package Type: XX = BV or ZS or Z
  BV = 48-ball VFBGA; ZS = 44-pin TSOP II; Z = 48-pin TSOP I
- Speed Grade: XX = 45 or 55
  45 = 45 ns; 55 = 55 ns
- Voltage Range: XX = 30 or 18
  30 = 3 V typ; 18 = 1.8 V typ
- ERR Output: Single-bit error correction indicator
- Process Technology: G = 65 nm
- Bus Width: 7 = × 16
- Density: 5 = 8-Mbit
- Family Code: 621 = MoBL SRAM family
- Company ID: CY = Cypress

Package Diagrams

Figure 14. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D		8.00 BSC	
E		6.00 BSC	
D1		5.25 BSC	
E1		3.75 BSC	
MD		8	
ME		6	
n		48	
Ø b	0.25	0.30	0.35
eE		0.75 BSC	
eD		0.75 BSC	
SD		0.375 BSC	
SE		0.375 BSC	

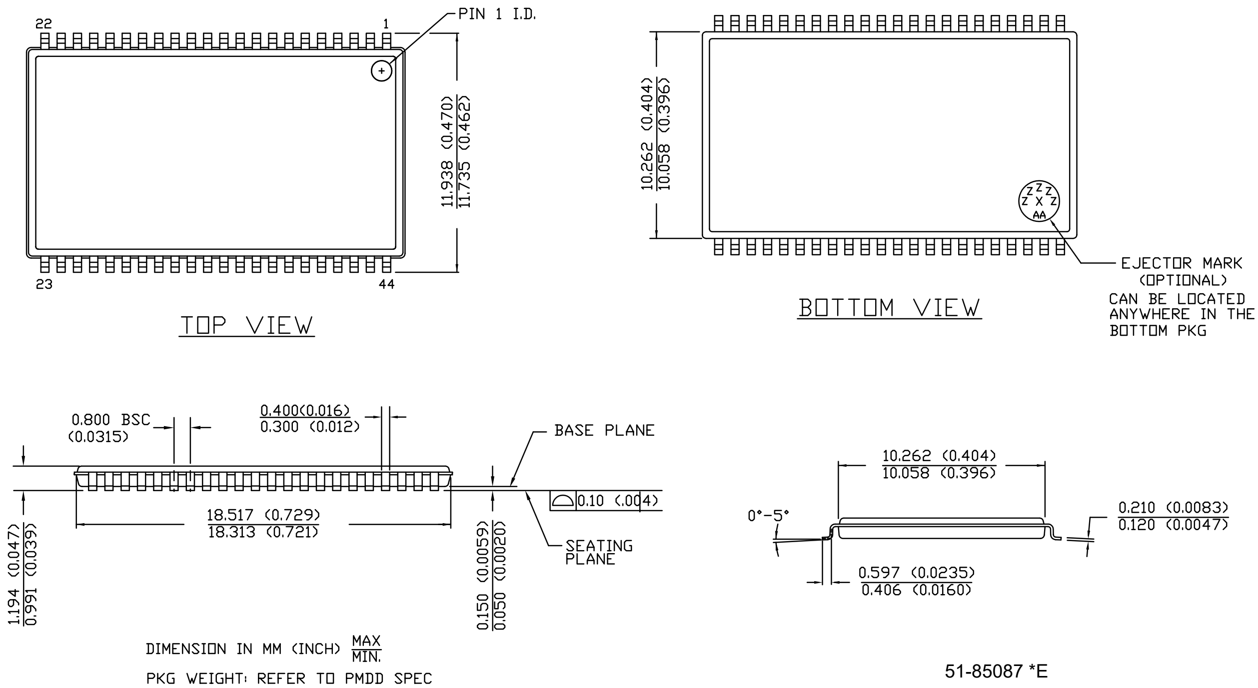
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

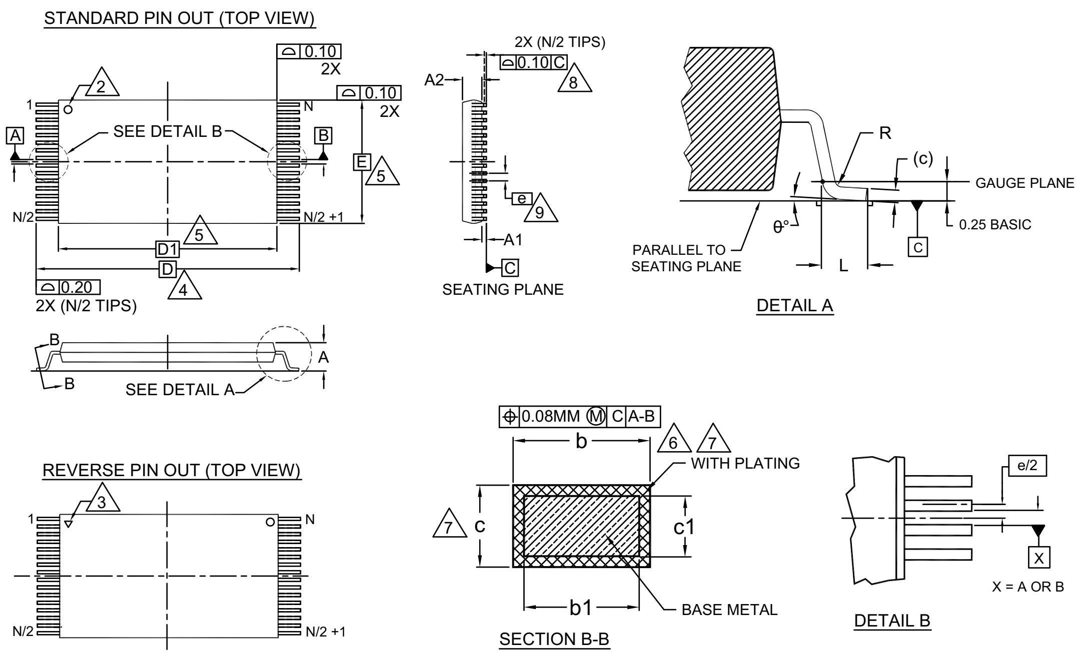
Package Diagrams (continued)

Figure 15. 44-pin TSOP II Package Outline, 51-85087



Package Diagrams (continued)

Figure 16. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Table 1. Acronyms used in this Document

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
ECC	error-correcting code
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TTL	transistor-transistor logic
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

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Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*C	6814364	02/28/2020	Release to web.

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