DRV871x-Q1 Automotive Multi-Channel Smart Half-Bridge Gate Drivers With Wide Common Mode Inline Current Sense Amplifiers

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Multi-channel half-bridge gate drivers
  - Pin to pin 4 and 8 half-bridge driver variants
  - 4.9V to 37V (40V abs. max) operating range
  - 4 PWM inputs with output mapping
  - Tripler charge pump for 100% PWM
  - Half-bridge, H-bridge, and SPI control modes
- Smart multi-stage gate drive architecture
  - Adjustable slew rate control
  - Adaptive propagation delay control
  - 50µA to 62mA peak source current output
  - 50µA to 62mA peak sink current output
  - Integrated dead-time handshaking
- 2x wide common mode current shunt amplifiers
  - Supports inline, high-side, or low-side
  - Adjustable gain settings (10, 20, 40, 80V/V)
- Multiple interface options available
  - SPI: Detailed configuration and diagnostics
  - H/W: Simplified control and less MCU pins
- Compact VQFN packages with wettable flanks
- Integrated protection features
  - Dedicated driver disable pin (DRVOFF)
  - Low I_Q, sleep mode motor braking (BRAKE)
  - Supply and regulator voltage monitors
  - MOSFET V_{DS} overcurrent monitors
  - MOSFET V_{GS} gate fault monitors
  - Charge pump for reverse polarity MOSFET
  - Offline open load and short circuit diagnostics
  - Device thermal warning and shutdown
  - Window watchdog timer
  - Fault condition interrupt pin (nFAULT)

2 Applications

- Automotive brushed DC motors
- Power seat modules
- Power trunk and lift gate
- Door module
- Body control modules
- Power sunroof
- Transmission and engine control modules

3 Description

The DRV871x-Q1 family of devices are highly integrated, multi-channel gate drivers intended for driving multiple motors or loads. The devices integrate either 4 (DRV8714-Q1) or 8 (DRV8718-Q1) half-bridge gate drivers, driver power supplies, current shunt amplifiers, and protection monitors reducing total system complexity, size, and cost.

A smart gate drive architecture manages dead time to prevent shoot-through, controls slew rate to decrease electromagnetic interference (EMI), and optimizes propagation delay for enhanced performance.

Input modes are provided for independent half-bridge or H-bridge control. Four PWM inputs can be multiplexed between the different drivers in combination with SPI control.

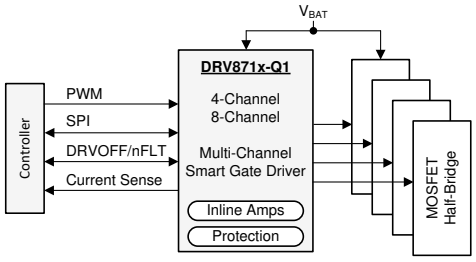
Wide common mode shunt amplifiers provide inline current sensing to continuously measure motor current even during recirculating windows. The amplifier can be used in low-side or high-side sense configurations if inline sensing is not required.

The devices provide an array of protection features to promote robust system operation. These include under and overvoltage monitors, V_{DS} overcurrent and V_{GS} gate fault monitors for the external MOSFETs, offline open load and short circuit diagnostics, and internal thermal warning and shutdown protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8714-Q1	VQFN (40)	6.00mm x 6.00mm
	HTQFP (48)	7.00mm x 7.00mm
	VQFN (56)	8.00mm x 8.00mm
DRV8718-Q1	VQFN (56)	8.00mm x 8.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simple Block Diagram

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4 Device Comparison Table

DEVICE	HALF-BRIDGES	AMPLIFIERS	INTERFACE	PACKAGE	PINS
DRV8714H-Q1	4	2	Hardware (H/W)	6x6mm VQFN	40
				7x7mm HTQFP	48
DRV8714S-Q1(1)	4	2	Serial (SPI)	6x6mm VQFN	40
				7x7mm HTQFP	48
				8x8mm VQFN	56
DRV8718S-Q1	8	2	Serial (SPI)	8x8mm VQFN	56

(1) The DRV8714A-Q1 (DRV8714SAQRHARQ1) is a variant of the DRV8714S-Q1 in the 6x6mm VQFN 40 pin package. The only electrical or functional difference is the change of the V_{POB_VDS} electrical threshold to 800mV.

Table 4-1. DRV8714-Q1 SPI vs. H/W Feature Comparison

Feature	DRV8714S-Q1 SPI Interface	DRV8714H-Q1 H/W Interface
PWM Input Mode	4 Modes	4 Modes
Gate Drive Output Current (I_{DRIVE})	16 Settings	6 Settings
Dead Time	Handshake + 3 Fixed Settings	Handshake Only
V_{DS} Comparator Threshold	16 Settings	6 Settings
V_{DS} and V_{GS} Blanking Time (t_{DRIVE})	8 Settings	Fixed, 8µs
V_{DS} Deglitch Time	4 Settings	Fixed, 4µs
V_{GS} Deglitch Time	Fixed, 2µs	Fixed, 2µs
V_{DS} Fault Response	4 Modes	Fixed, Cycle-By-Cycle
V_{GS} Fault Response	4 Modes	Fixed, Cycle-By-Cycle
Amplifier Gain	4 Settings	4 Settings
Amplifier Blanking Time	8 Settings	N/A
Amplifier Reference Voltage	2 Settings	Fixed, V_{AREF} / 2
V_{PVDD} Undervoltage Fault Response	2 Modes	Auto Retry
V_{PVDD} Overvoltage Fault Response	4 Modes	N/A
V_{VCP} Undervoltage Fault Response	2 Modes	Auto Retry
V_{VCP} Undervoltage Threshold	2 Settings	Fixed, 2.5V
Offline Open Load Diagnostic	Available	N/A
Offline Short Circuit Diagnostic	Available	N/A
Watchdog Timer	Available	N/A
Multi-Function DRVOFF/nFLT Pin	Configurable DRVOFF or nFLT	nFLT Fault Report Only

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5 Pin Configuration and Functions

5.1 VQFN (RVJ) 56-Pin Package and Pin Functions

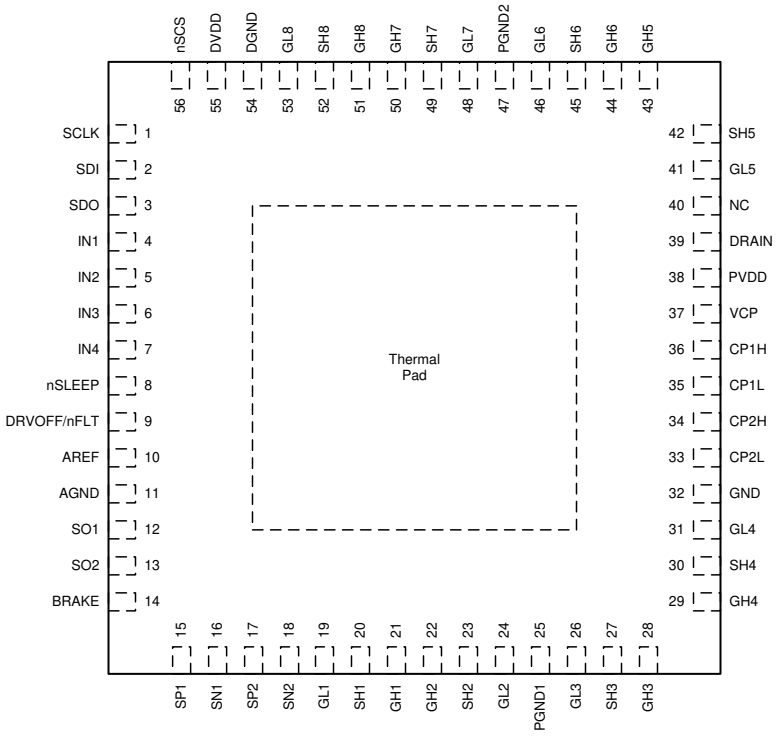

Figure 5-1. DRV8718S-Q1 VQFN (RVJ) 56-Pin Package Top View

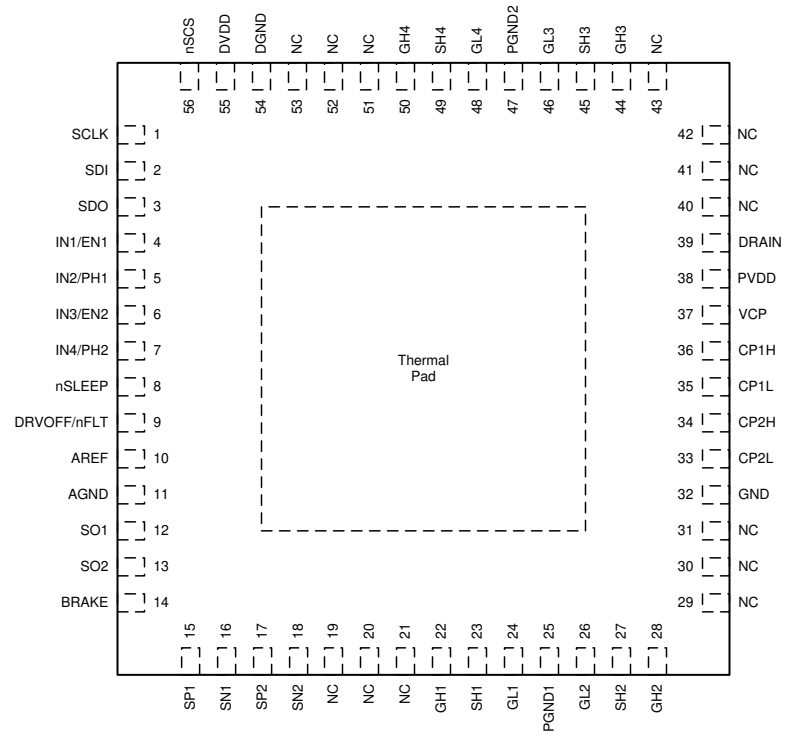

Figure 5-2. DRV8714S-Q1 VQFN (RVJ) 56-Pin Package Top View

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Table 5-1. VQFN (RVJ) 56-Pin Package Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NO.	NAME				
	DRV8718S-Q1	DRV8714S-Q1			
1	SCLK		I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pulldown resistor.
2	SDI		I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor.
3	SDO		O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
4	IN1	IN1/EN1	I	Digital	Half-bridge and H-bridge control input. See Section 7.3.3. Internal pulldown.
5	IN2	IN2/PH1	I	Digital	
6	IN3	IN3/EN2	I	Digital	
7	IN4	IN4/PH2	I	Digital	
8	nSLEEP		I	Digital	Device enable pin. Logic low to shutdown the device and enter sleep mode. Internal pulldown resistor.
9	DRVOFF/nFLT		I/O	Digital	Multi-function pin for either driver shutdown input or fault indicator output. See Section 7.3.8. Internal pulldown resistor.
10	AREF		I	Power	External voltage reference and power supply for current sense amplifiers. Recommended to connect a 0.1µF, 6.3V ceramic capacitor between the AREF and AGND pins.
11	AGND		I/O	Power	Device ground. Connect to system ground.
12	SO1		O	Analog	Shunt amplifier output.
13	SO2		O	Analog	Shunt amplifier output.
14	BRAKE		I	Digital	Powered off braking pin. Logic high to enable low-side gate drivers while in low-power sleep mode. See Section 7.3.8.2. Internal pulldown resistor.
15	SP1		I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
16	SN1		I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
17	SP2		I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
18	SN2		I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
19	GL1	NC	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
20	SH1	NC	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
21	GH1	NC	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
22	GH2	GH1	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
23	SH2	SH1	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
24	GL2	GL1	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
25	PGND1		I	Analog	Low-side MOSFET gate drive 1-4 sense and power return. Connect to system ground close to the device and half-bridge 1-4.
26	GL3	GL2	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
27	SH3	SH2	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
28	GH3	GH2	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
29	GH4	NC	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
30	SH4	NC	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
31	GL4	NC	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
32	GND		I/O	Ground	Device ground. Connect to system ground.
33	CP2L		I/O	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between the CP2H and CP2L pins.
34	CP2H		I/O	Power	
35	CP1L		I/O	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between the CP1H and CP1L pins.
36	CP1H		I/O	Power	

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Table 5-1. VQFN (RVJ) 56-Pin Package Pin Functions (continued)

PIN			I/O	TYPE	DESCRIPTION
NO.	NAME				
	DRV8718S-Q1	DRV8714S-Q1			
37	VCP		I/O	Power	Charge pump output. Connect a 1µF, 16V ceramic capacitor between the VCP and PVDD pins.
38	PVDD		I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10µF between PVDD and GND pins.
39	DRAIN		I	Analog	Bridge MOSFET drain voltage sense pin. Connect to common point of the high-side MOSFET drains.
40	NC		—	—	No connection.
41	GL5	NC	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
42	SH5	NC	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
43	GH5	NC	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
44	GH6	GH3	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
45	SH6	SH3	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
46	GL6	GL3	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
47	PGND2		I	Analog	Low-side MOSFET gate drive 5-8 sense and power return. Connect to system ground close to the device and half-bridge 5-8.
48	GL7	GL4	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
49	SH7	SH4	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
50	GH7	GH4	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
51	GH8	NC	O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
52	SH8	NC	I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
53	GL8	NC	O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
54	DGND		I/O	Ground	Device ground. Connect to system ground.
55	DVDD		I	Power	Device logic and digital output power supply input. Recommended to connect a 1.0µF, 6.3V ceramic capacitor between the DVDD and GND pins.
56	nSCS		I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor.

Note

The DRV8718-Q1 56-Pin VQFN (RVJ) and DRV8714-Q1 56-Pin VQFN (RVJ) packages are drop in pin-to-pin compatible. Please note that the locations of half-bridges 1,2,3 and 4 are shifted for the DRV8714-Q1 to help with PCB routing.

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5.2 VQFN (RHA) 40-Pin Package and Pin Functions

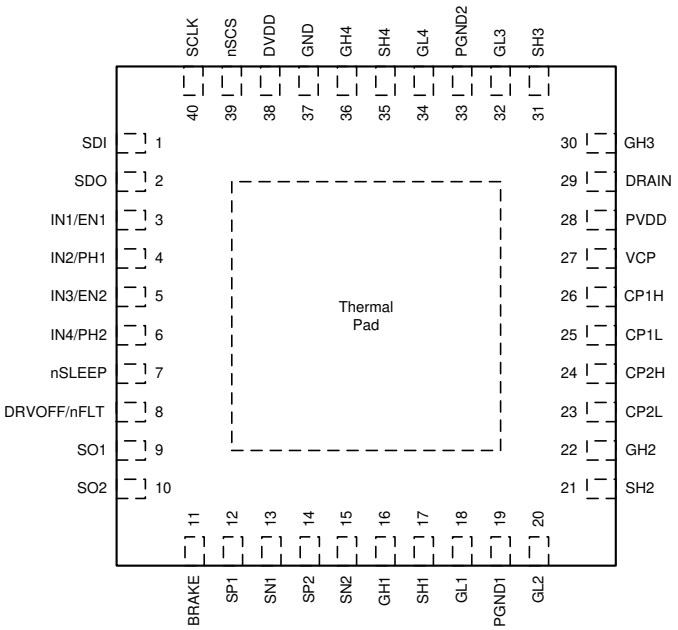

Figure 5-3. DRV8714S-Q1 VQFN (RHA) 40-Pin Package Top View

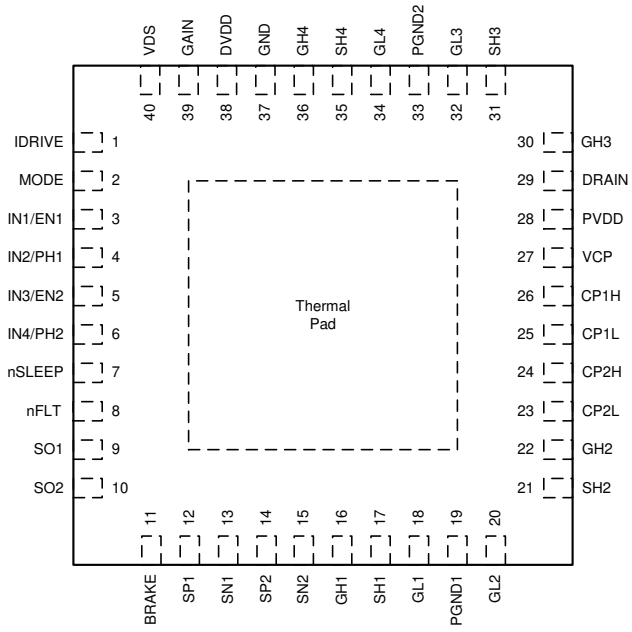

Figure 5-4. DRV8714H-Q1 VQFN (RHA) 40-Pin Package Top View

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Table 5-2. VQFN (RHA) 40-Pin Package Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NO.	NAME				
	DRV8714S-Q1	DRV8714H-Q1			
1	SDI	—	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor.
	—	IDRIVE	I	Analog	Gate driver output current setting. 6 level input pin set by an external resistor.
2	SDO	—	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
	—	MODE	I	Analog	Analog PWM input mode setting. 4 level input pin set by an external resistor.
3	IN1/EN1		I	Digital	Half-bridge and H-bridge control input. See Section 7.3.3. Internal pulldown.
4	IN2/PH1		I	Digital	
5	IN3/EN2		I	Digital	
6	IN4/PH2		I	Digital	
7	nSLEEP		I	Digital	Device enable pin. Logic low to shutdown the device and enter sleep mode. Internal pulldown resistor.
8	DRVOFF/nFLT	—	I/O	Digital	Multi-function pin for either driver shutdown input or fault indicator output. See Section 7.3.8. Internal pulldown resistor.
	—	nFLT	O	Digital	Fault indicator output. This pin is pulled logic low to indicate a fault condition. Open-drain output. Requires external pullup resistor.
9	SO1		O	Analog	Shunt amplifier output.
10	SO2		O	Analog	Shunt amplifier output.
11	BRAKE		I	Digital	Powered off braking pin. Logic high to enable low-side gate drivers while in low-power sleep mode. See Section 7.3.8.2. Internal pulldown resistor.
12	SP1		I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
13	SN1		I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
14	SP2		I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
15	SN2		I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
16	GH1		O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
17	SH1		I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
18	GL1		O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
19	PGND1		I	Analog	Low-side MOSFET gate drive 1-2 sense and power return. Connect to system ground close to the device and half-bridge 1-2.
20	GL2		O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
21	SH2		I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
22	GH2		O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
23	CP2L		I/O	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between the CP2H and CP2L pins.
24	CP2H		I/O	Power	
25	CP1L		I/O	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between the CP1H and CP1L pins.
26	CP1H		I/O	Power	
27	VCP		I/O	Power	Charge pump output. Connect a 1µF, 16V ceramic capacitor between the VCP and PVDD pins.
28	PVDD		I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10µF between PVDD and GND pins.
29	DRAIN		I	Analog	Bridge MOSFET drain voltage sense pin. Connect to common point of the high-side MOSFET drains.
30	GH3		O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
31	SH3		I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
32	GL3		O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.

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Table 5-2. VQFN (RHA) 40-Pin Package Pin Functions (continued)

PIN			I/O	TYPE	DESCRIPTION
NO.	NAME				
	DRV8714S-Q1	DRV8714H-Q1			
33	PGND2		I	Analog	Low-side MOSFET gate drive 3-4 sense and power return. Connect to system ground close to the device and half-bridge 3-4.
34	GL4		O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
35	SH4		I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
36	GH4		O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
37	GND		I/O	Ground	Device ground. Connect to system ground.
38	DVDD		I	Power	Device logic and digital output power supply input. External voltage reference and power supply for current sense amplifiers. Recommended to connect a 1.0µF, 6.3V ceramic capacitor between the DVDD and GND pins.
39	nSCS	—	I	Digital	Serial chip select. A logic low on this pin enables serial interface communication. Internal pullup resistor.
	—	GAIN	I	Analog	Amplifier gain setting. 4 level input pin set by an external resistor.
40	SCLK	—	I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pulldown resistor.
	—	VDS	I	Analog	VDS monitor threshold setting. 6 level input pin set by an external resistor.

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5.3 HTQFP (PHP) 48-Pin Package and Pin Functions

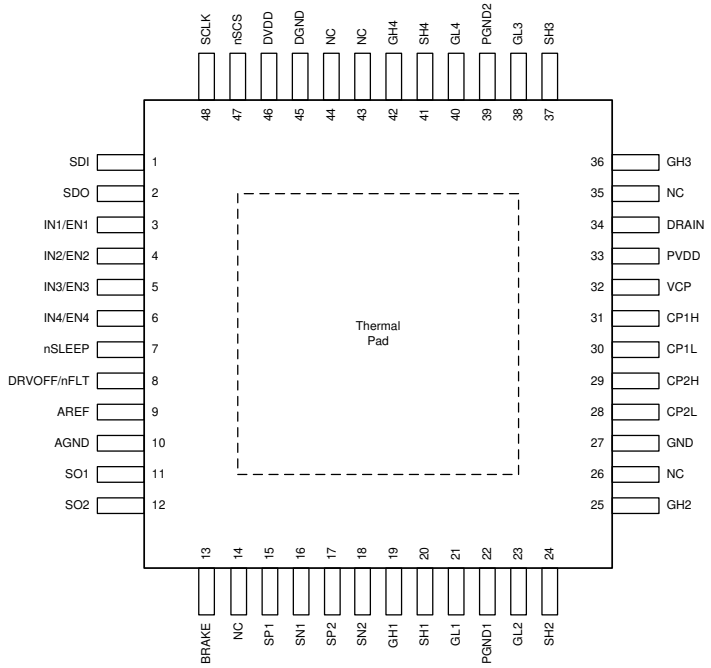

Figure 5-5. DRV8714S-Q1 HTQFP (PHP) 48-Pin Package Top View

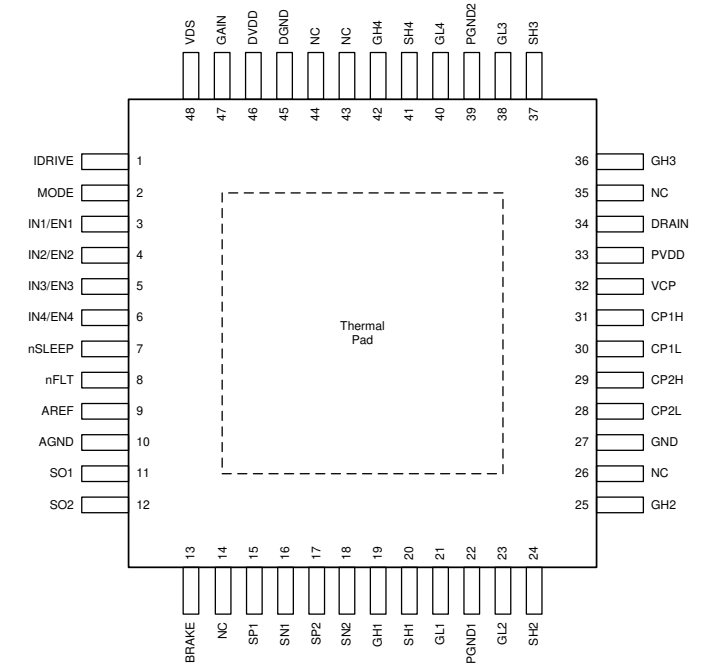

Figure 5-6. DRV8714H-Q1 HTQFP (PHP) 48-Pin Package Top View

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Table 5-3. HTQFP (PHP) 48-Pin Package Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NO.	NAME				
	DRV8714S-Q1	DRV8714H-Q1			
1	SDI	—	I	Digital	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pulldown resistor.
	—	IDRIVE	I	Analog	Gate driver output current setting. 6 level input pin set by an external resistor.
2	SDO	—	O	Digital	Serial data output. Data is shifted out on the rising edge of the SCLK pin. Push-pull output.
	—	MODE	I	Analog	Analog PWM input mode setting. 4 level input pin set by an external resistor.
3	IN1/EN1		I	Digital	Half-bridge and H-bridge control input. See Section 7.3.3. Internal pulldown.
4	IN2/PH1		I	Digital	
5	IN3/EN2		I	Digital	
6	IN4/PH2		I	Digital	
7	nSLEEP		I	Digital	Device enable pin. Logic low to shutdown the device and enter sleep mode. Internal pulldown resistor.
8	DRVOFF/nFLT	—	I/O	Digital	Multi-function pin for either driver shutdown input or fault indicator output. See Section 7.3.8. Internal pulldown resistor.
	—	nFLT	O	Digital	Fault indicator output. This pin is pulled logic low to indicate a fault condition. Open-drain output. Requires external pullup resistor.
9	AREF		I	Power	External voltage reference and power supply for current sense amplifiers. Recommended to connect a 0.1µF, 6.3V ceramic capacitor between the AREF and AGND pins.
10	AGND		I/O	Power	Device ground. Connect to system ground.
11	SO1		O	Analog	Shunt amplifier output.
12	SO2		O	Analog	Shunt amplifier output.
13	BRAKE		I	Digital	Powered off braking pin. Logic high to enable low-side gate drivers while in low-power sleep mode. See Section 7.3.8.2. Internal pulldown resistor.
14	NC		—	—	No connection.
15	SP1		I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
16	SN1		I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
17	SP2		I	Analog	Amplifier positive input. Connect to positive terminal of the shunt resistor.
18	SN2		I	Analog	Amplifier negative input. Connect to negative terminal of the shunt resistor.
19	GH1		O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
20	SH1		I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
21	GL1		O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
22	PGND1		I	Analog	Low-side MOSFET gate drive 1-2 sense and power return. Connect to system ground close to the device and half-bridge 1-2.
23	GL2		O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
24	SH2		I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
25	GH2		O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
26	NC		—	—	No connection.
27	GND		I/O	Power	Device ground. Connect to system ground.
28	CP2L		I/O	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between the CP2H and CP2L pins.
29	CP2H		I/O	Power	
30	CP1L		I/O	Power	Charge pump switching node. Connect a 100nF, PVDD-rated ceramic capacitor between the CP1H and CP1L pins.
31	CP1H		I/O	Power	
32	VCP		I/O	Power	Charge pump output. Connect a 1µF, 16V ceramic capacitor between the VCP and PVDD pins.

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Table 5-3. HTQFP (PHP) 48-Pin Package Pin Functions (continued)

PIN			I/O	TYPE	DESCRIPTION
NO.	NAME				
	DRV8714S-Q1	DRV8714H-Q1			
33	PVDD		I	Power	Device driver power supply input. Connect to the bridge power supply. Connect a 0.1µF, PVDD-rated ceramic capacitor and local bulk capacitance greater than or equal to 10µF between PVDD and GND pins.
34	DRAIN		I	Analog	Bridge MOSFET drain voltage sense pin. Connect to common point of the high-side MOSFET drains.
35	NC		—	—	No connection.
36	GH3		O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
37	SH3		I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
38	GL3		O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
39	PGND2		I	Analog	Low-side MOSFET gate drive 3-4 sense and power return. Connect to system ground close to the device and half-bridge 3-4.
40	GL4		O	Analog	Low-side gate driver output. Connect to the gate of the low-side MOSFET.
41	SH4		I	Analog	High-side source sense input. Connect to the high-side MOSFET source.
42	GH4		O	Analog	High-side gate driver output. Connect to the gate of the high-side MOSFET.
43	NC		—	—	No connection.
44	NC		—	—	No connection.
45	DGND		I/O	Ground	Device ground. Connect to system ground.
46	DVDD		I	Power	Device logic and digital output power supply input. External voltage reference and power supply for current sense amplifiers. Recommended to connect a 1.0µF, 6.3V ceramic capacitor between the DVDD and GND pins.
47	nSCS	—	I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pullup resistor.
	—	GAIN	I	Analog	Amplifier gain setting. 4 level input pin set by an external resistor.
48	SCLK	—	I	Digital	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pulldown resistor.
	—	VDS	I	Analog	VDS monitor threshold setting. 6 level input pin set by an external resistor.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Driver power supply pin voltage	PVDD	–0.3	40	V
MOSFET drain sense pin voltage	DRAIN	–0.3	40	V
Voltage difference between ground pins	AGND, DGND, GND	–0.3	0.3	V
Charge pump pin voltage	VCP	–0.3	55	V
Charge pump high-side pin voltage	CP1H	V_{PVDD} – 0.3	V_{VCP} + 0.3	V
	CP2H	V_{PVDD} – 0.6	V_{VCP} + 0.3	V
Charge pump low-side pin voltage	CP1L, CP2L	–0.3	V_{PVDD} + 0.3	V
Digital power supply pin voltage	DVDD	–0.3	5.75	V
Logic pin voltage	DRVOFF/nFLT, GAIN, IDRIVE, INx/ENx, INx/PHx, MODE, nSLEEP, nSCS, SCLK, SDI, VDS	–0.3	5.75	V
Output logic pin voltage	DRVOFF/nFLT, SDO	–0.3	V_{DVDD} + 0.3	V
Brake pin voltage	BRAKE	–0.3	V_{PVDD} + 0.3	V
High-side gate drive pin voltage	GHx(2)	–2	V_{VCP} + 0.3	V
Transient 1-µs high-side gate drive pin voltage		–5	V_{VCP} + 0.3	
High-side gate drive pin voltage with respect to SHx		–0.3	13.5	
High-side sense pin voltage	SHx(2)	–2	40	V
Transient 1-µs high-side sense pin voltage		–5	40	
Low-side gate drive pin voltage	GLx(2)	–2	13.5	V
Transient 1-µs low-side gate drive pin voltage		–3	13.5	
Low-side gate drive pin voltage with respect to PGNDx		–0.3	13.5	
Low-side sense pin voltage	PGNDx(2)	–2	2	V
Transient 1-µs low-side sense pin voltage		–3	3	
Peak gate drive current	GHx, GLx	Internally Limited	Internally Limited	mA
Amplfier power supply and reference pin voltage	AREF	–0.3	5.75	V
Amplifier input pin voltage	SNx, SPx	–2	V_{VCP} + 0.3	V
Transient 1-µs amplifier input pin voltage		–5	V_{VCP} + 0.3	
Amplifier input differential voltage	SNx, SPx	–5.75	5.75	V
Amplifier output pin voltage	SOx	–0.3	V_{AREF} + 0.3	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) PVDD and DRAIN with respect to GHx, SHx, GLx, or PGNDx should not exceed 40-V. When PVDD or DRAIN are greater than 35-V, negative voltage on GHx, SHx, GLx, and PGNDx should be limited to ensure this rating is not exceeded. When PVDD and DRAIN are less than 35-V, the full negative voltage rating of GHx, SHx, GLx, and PGNDx is available.

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6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVDD}	Driver power supply voltage	PVDD	4.9		37	V
I_{HS} (1)	High-side average gate-drive current	GHx	0		15	mA
I_{LS} (1)	Low-side average gate-drive current	GLx	0		15	mA
V_{DVDD}	Digital power supply voltage	DVDD	3		5.5	V
V_{DIN}	Digital input voltage	BRAKE, DRVOFF/nFLT, INx/ENx, INx/PHx, nSLEEP, nSCS, SCLK, SDI	0		5.5	V
I_{DOUT}	Digital output current	SDO	0		5	mA
V_{OD}	Open drain pullup voltage	DRVOFF/nFLT	0		5.5	V
I_{OD}	Open drain output current	DRVOFF/nFLT	0		5	mA
V_{BRAKE}	Brake input voltage	BRAKE	0		PVDD	V
V_{AREF}	Amplfier reference supply voltage	AREF	3		5.5	V
I_{SO}	Shunt amplifier output current	SOx	0		5	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC[1]		DRV8718-Q1 RVJ (VQFN) 56 PINS	DRV8714-Q1 RVJ (VQFN) 56 PINS	DRV8714-Q1 RHA (VQFN) 40 PINS	DRV8714-Q1 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.6	24.7	31	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.2	14.1	20.9	18.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.0	9.0	12.5	13.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	0.2	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.9	9.0	12.4	13.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.0	2.3	2.3	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DRAIN, DVDD, PVDD, VCP)					

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4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 0 V BRAKE = 0 V, –40 ≤ T_J ≤ 85°C		2.25	3.5	µA
		V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 0 V BRAKE = 5 V, –40 ≤ T_J ≤ 85°C		10	15	µA
I_{DRAINQ}	DRAIN sleep mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 0 V –40 ≤ T_J ≤ 85°C		1.25	2	µA
I_{DVDDQ}	DVDD sleep mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 0 V –40 ≤ T_J ≤ 85°C		1.25	3	µA
		V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 0 V –40 ≤ T_J ≤ 85°C, DRV8714-Q1 RHA		2.25	5.25	
I_{PVDD}	PVDD active mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 5 V		13.5	15.5	mA
I_{DRAIN}	DRAIN active mode current	V_{PVDD}, V_{DRAIN} = 13.5 V, nSLEEP = 5 V, V_{DS_LVL} ≤ 500 mV		1	1.65	mA
I_{DVDD}	DVDD active mode current	V_{DVDD} = 5 V, SDO = 0 V DRV8718-Q1 RVJ, DRV8714-Q1 RVJ		8	10	mA
		V_{DVDD} = 5 V, SDO = 0 V DRV8714-Q1 RHA		10	13	mA
f_{DVDD}	Digital oscilator switching frequency	Primary frequency of spread spectrum.		14.25		MHz
t_{WAKE}	Turnon time	nSLEEP = 5 V to active mode			1	ms
t_{SLEEP}	Turnoff time	nSLEEP = 0 V to sleep mode			1	ms
V_{VCP}	Charge pump regulator voltage with respect to PVDD Triple mode	V_{PVDD} ≥ 9 V, I_{VCP} ≤ 30 mA	9.5	10.5	11	V
		V_{PVDD} = 7 V, I_{VCP} ≤ 25 mA	8.5	9	11	
		V_{PVDD} = 7 V, I_{VCP} ≤ 25 mA, DRV8714-Q1 RHA	8.4	9	11	
		V_{PVDD} = 4.9 V, I_{VCP} ≤ 12 mA	7	7.5	11	
		V_{PVDD} = 4.9 V, I_{VCP} ≤ 12 mA, DRV8714-Q1 RHA	6.8	7.5	11	
	Charge pump regulator voltage with respect to PVDD Double mode	V_{PVDD} ≥ 13 V, I_{VCP} ≤ 25 mA	9.5	10.5	11	V
		V_{PVDD} = 9 V, I_{VCP} ≤ 13.5 mA	7	8	11	
		V_{PVDD} = 9 V, I_{VCP} ≤ 13.5 mA, DRV8714-Q1 RHA	6.9	8	11	
		V_{PVDD} = 7 V, I_{VCP} ≤ 10 mA	5.4	6	11	
		V_{PVDD} = 7 V, I_{VCP} ≤ 10 mA, DRV8714-Q1 RHA	5.3	6	11	
f_{VCP}	Charge pump switching frequency	Primary frequency of spread spectrum.		400		kHz
LOGIC-LEVEL INPUTS (BRAKE, DRVOFF/nFLT, INx/EN, INx/PHx, nSLEEP, nSCS, SCLK, SDI)						
V_{IL}	Input logic low voltage	DRVOFF/nFLT, INx/ENx, INx/PHx, nSLEEP, SCLK, SDI	0		V_{DVDD} x 0.3	V
		BRAKE	0		0.6	
V_{IH}	Input logic high voltage	DRVOFF/nFLT, INx/ENx, INx/PHx, nSLEEP, SCLK, SDI	V_{DVDD} x 0.7		5.5	V
		BRAKE	1.8		5.5	
V_{HYS}	Input hysteresis	DRVOFF/nFLT, INx/ENx, INx/PHx, nSLEEP, SCLK, SDI		V_{DVDD} x 0.1		V
		BRAKE		0.5		
I_{IL}	Input logic low current	V_{DIN} = 0 V, BRAKE, DRVOFF/nFLT, INx/ENx, INx/PHx, nSLEEP, SCLK, SDI	–5		5	µA
		V_{DIN} = 0 V, nSCS		50	100	

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4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic high current	V_{DIN} = 5 V, DRVOFF/nFLT, INx/ENx, INx/PHx, nSLEEP, SCLK, SDI		50	100	µA
		V_{DIN} = 5 V, V_{DVDD} = 5 V, nSCS	–5		5	
		V_{DIN} = 5 V, nSLEEP = 0V, BRAKE		5	10	µA
		V_{DIN} = 5 V, nSLEEP = 5V, BRAKE		35	100	µA
R_{PD}	Input pulldown resistance	To GND, DRVOFF/nFLT, INx/ENx, INx/PHx, nSLEEP, SCLK, SDI	50	100	150	kΩ
		BRAKE to GND, nSLEEP = 0 V BRAKE ≤ 2 V, 4.9 V ≤ V_{PVDD} ≤ V_{POB_OV}	500	1000	1500	kΩ
		BRAKE to GND, nSLEEP = 5 V BRAKE ≤ 2 V, 4.9 V ≤ V_{PVDD} ≤ V_{POB_OV}	50	136	200	kΩ
R_{PU}	Input pullup resistance	To DVDD, nSCS	50	100	150	kΩ
MULTI-LEVEL INPUTS (GAIN, IDRIVE, MODE, VDS)						
V_{QI1}	Quad-level input 1	GAIN, MODE Voltage to set level 1	0		V_{DVDD} x 0.1	V
R_{QI2}	Quad-level input 2	GAIN, MODE Resistance to GND to set level 2	44.65	47	49.35	kΩ
R_{QI3}	Quad-level input 3	GAIN, MODE Resistance to GND to set level 3	500	Hi-Z		kΩ
V_{QI4}	Quad-level input 4	GAIN, MODE Voltage to set level 4	V_{DVDD} x 0.9		5.5	V
R_{QPD}	Quad-level pulldown resistane	To GND, GAIN, MODE		98		kΩ
R_{QPU}	Quad-level pullup resistane	To DVDD, GAIN, MODE		98		kΩ
V_{SI1}	Six-level input 1	IDRIVE, VDS Voltage to set level 1	0		V_{DVDD} x 0.1	V
R_{SI2}	Six-level input 2	IDRIVE, VDS Resistance to GND to set level 2	28.5	30	31.5	kΩ
R_{SI3}	Six-level input 3	IDRIVE, VDS Resistance to GND to set level 3	95	100	105	kΩ
R_{SI4}	Six-level input 4	IDRIVE, VDS Resistance to GND to set level 4	500	Hi-Z		kΩ
R_{SI5}	Six-level input 5	IDRIVE, VDS Resistance to DVDD to set level 5	58.9	62	65.1	kΩ
R_{SI6}	Six-level input 6	IDRIVE, VDS Voltage to set level 6	V_{DVDD} x 0.9		5.5	V
R_{SPD}	Six-level pulldown resistane	To GND, IDRIVE, VDS		98		kΩ
R_{SPU}	Six-level pullup resistane	To DVDD, IDRIVE, VDS		69		kΩ
LOGIC-LEVEL OUTPUTS (DRVOFF/nFLT, SDO)						
V_{OL}	Output logic low voltage	I_{DOUT} = 5 mA			0.5	V
V_{OH}	Output logic high voltage	I_{DOUT} = –5 mA, SDO	V_{DVDD} x 0.8			V
I_{ODZ}	Open-drain logic high current	V_{OD} = 5 V, DRVOFF/nFLT	–10		10	µA
GATE DRIVERS (GHx, GLx)						
V_{GHx_L}	GHx low level output voltage	I_{DRVN_HS} = I_{STRONG}, I_{GHx} = 1mA, GHx to SHx	0		0.25	V
V_{GLx_L}	GLx low level output voltage	I_{DRVN_LS} = I_{STRONG}, I_{GLx} = 1mA, GLx to PGNDx	0		0.25	V
V_{GHx_H}	GHx high level output voltage	I_{DRVP_HS} = I_{HOLD}, I_{GHx} = 1mA, VCP to GHx	0		0.25	V
V_{GLx_H}	GLx high level output voltage	I_{DRVP_LS} = I_{HOLD}, I_{GLx} = 1mA, GLx to PGNDx		10.5	12.5	V

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4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DRVP, SPI}$	Peak gate current (source) SPI Device	IDRVP_x = 0000b, V_{GSx} = 3 V	0.2	0.5	0.83	mA
		IDRVP_x = 0001b, V_{GSx} = 3 V	0.5	1	1.6	
		IDRVP_x = 0010b, V_{GSx} = 3 V	1.3	2	2.8	
		IDRVP_x = 0011b, V_{GSx} = 3 V	2.1	3	4	
		IDRVP_x = 0100b, V_{GSx} = 3 V	2.9	4	5.3	
		IDRVP_x = 0101b, V_{GSx} = 3 V	3.75	5	6.4	
		IDRVP_x = 0110b, V_{GSx} = 3 V	4.5	6	7.6	
		IDRVP_x = 0111b, V_{GSx} = 3 V	5.5	7	9	
		IDRVP_x = 1000b, V_{GSx} = 3 V	6	8	10	
		IDRVP_x = 1001b, V_{GSx} = 3 V	9	12	15	
		IDRVP_x = 1010b, V_{GSx} = 3 V	12	16	20	
		IDRVP_x = 1011b, V_{GSx} = 3 V	15	20	25	
		IDRVP_x = 1100b, V_{GSx} = 3 V	18	24	30	
		IDRVP_x = 1101b, V_{GSx} = 3 V	24	31	40	
		IDRVP_x = 1110b, V_{GSx} = 3 V	28	48	62	
		IDRVP_x = 1111b, V_{GSx} = 3 V	46	62	78	
$I_{DRVP, H/W}$	Peak gate current (source) H/W Device	IDRIVE six-level 1, V_{GSx} = 3 V	0.2	1	1.6	mA
		IDRIVE six-level 2, V_{GSx} = 3 V	2.9	4	5.3	
		IDRIVE six-level 3, V_{GSx} = 3 V	6	8	10	
		IDRIVE six-level 4, V_{GSx} = 3 V	12	16	20	
		IDRIVE six-level 5, V_{GSx} = 3 V	24	31	40	
		IDRIVE six-level 6, V_{GSx} = 3 V	46	62	78	
$I_{DRVN, SPI}$	Peak gate current (sink) SPI Device	IDRVN_x = 0000b, V_{GSx} = 3 V	0.07	0.5	0.85	mA
		IDRVN_x = 0001b, V_{GSx} = 3 V	0.23	1	1.7	
		IDRVN_x = 0010b, V_{GSx} = 3 V	0.7	2	3.2	
		IDRVN_x = 0011b, V_{GSx} = 3 V	1.2	3	4.6	
		IDRVN_x = 0100b, V_{GSx} = 3 V	1.75	4	5.9	
		IDRVN_x = 0101b, V_{GSx} = 3 V	2.4	5	7.2	
		IDRVN_x = 0110b, V_{GSx} = 3 V	3	6	8.5	
		IDRVN_x = 0111b, V_{GSx} = 3 V	3.6	7	9.8	
		IDRVN_x = 1000b, V_{GSx} = 3 V	4.3	8	11	
		IDRVN_x = 1001b, V_{GSx} = 3 V	7.3	12	16	
		IDRVN_x = 1010b, V_{GSx} = 3 V	11	16	20	
		IDRVN_x = 1011b, V_{GSx} = 3 V	14.3	20	25	
		IDRVN_x = 1100b, V_{GSx} = 3 V	18	24	30	
		IDRVN_x = 1101b, V_{GSx} = 3 V	24	31	40	
		IDRVN_x = 1110b, V_{GSx} = 3 V	28	48	62	
		IDRVN_x = 1111b, V_{GSx} = 3 V	46	62	78	
$I_{DRVN, H/W}$	Peak gate current (sink) H/W Device	IDRIVE six-level 1, V_{GSx} = 3 V	0.23	1	1.7	mA
		IDRIVE six-level 2, V_{GSx} = 3 V	1.75	4	5.9	
		IDRIVE six-level 3, V_{GSx} = 3 V	4.3	8	11	
		IDRIVE six-level 4, V_{GSx} = 3 V	11	16	20	
		IDRIVE six-level 5, V_{GSx} = 3 V	24	31	40	
		IDRIVE six-level 6, V_{GSx} = 3 V	46	62	78	
I_{HOLD}	Gate pullup hold current	Gate hold source current, V_{GSx} = 3 V	5	16	30	mA

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4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{STRONG}	Gate pulldown strong current	Gate strong pulldown current, V_{GSx} = 3 V I_{DRV} = 0.5 to 12mA	30	62	100	mA
		Gate strong pulldown current, V_{GSx} = 3 V I_{DRV} = 16 to 62mA	45	128	205	
R_{PDSA_LS}	Low-side semi-active gate pulldown	GLx to PGNDx, V_{GSx} = 3 V		1.8		kΩ
		GLx to PGNDx, V_{GSx} = 1 V		5		kΩ
R_{PD_HS}	High-side passive gate pulldown resistor	GHx to SHx		150		kΩ
R_{PD_LS}	Low-side passive gate pulldown resistor	DRV8718-Q1, GL1, GL2, GL3, and GL4 to PGND1		150		kΩ
I_{SHx}	Switch-node sense leakage current	Into SHx, SHx = DRAIN ≤ 28 V GHx – SHx = 0 V, nSLEEP = 0 V	–5	0	20	µA
		Into SHx, SHx = DRAIN ≤ 37 V GHx – SHx = 0 V, nSLEEP = 0 V	–5	0	80	µA
		Into SHx, SHx = DRAIN ≤ 37 V GHx – SHx = 0 V, nSLEEP = 5 V	–150	–100	0	µA
GATE DRIVER TIMINGS (GHx, GLx)						
t_{PDR_LS}	Low-side rising propagation delay	Input to GLx rising		300	850	ns
t_{PDF_LS}	Low-side falling propagation delay	Input to GLx falling		300	600	ns
t_{PDR_HS}	High-side rising propagation delay	Input to GHx rising		300	600	ns
t_{PDF_HS}	High-side falling propagation delay	Input to GHx falling		300	600	ns
t_{DEAD}	Internal handshake dead-time	GLx/GHx falling 10% to GHx/GLx rising 10%		350		ns
$t_{DEAD_D,\ SPI}$	Insertable digital dead-time SPI Device	VGS_TDEAD = 00b, Handshake only		0		µs
		VGS_TDEAD = 01b	1.6	2	2.4	
		VGS_TDEAD = 10b	3.4	4	4.6	
		VGS_TDEAD = 11b	7.2	8	8.8	
$t_{DEAD_D,\ H/W}$	Insertable digital dead-time H/W Device	Handshake only		0		µs
CURRENT SHUNT AMPLIFIERS (AREF, SNx, SOx, SPx)						
V_{COM}	Common mode input range		–2		V_{PVDD} + 2	V
$G_{CSA,\ SPI}$	Sense amplifier gain SPI device	CSA_GAIN = 00b	9.75	10	10.25	V/V
		CSA_GAIN = 01b	19.5	20	20.5	
		CSA_GAIN = 10b	39	40	41	
		CSA_GAIN = 11b	78	80	82	
$G_{CSA,\ H/W}$	Sense amplifier gain H/W device	GAIN quad-level 1	9.75	10	10.25	V/V
		GAIN quad-level 2	19.5	20	20.5	
		GAIN quad-level 3	39	40	41	
		GAIN quad-level 4	78	80	82	
t_{SET}	Sense amplifier settling time to ±1%	V_{SO_STEP} = 1.5 V, G_{CSA} = 10 V/V C_{SO} = 60 pF		2.2		µs
		V_{SO_STEP} = 1.5 V, G_{CSA} = 20 V/V C_{SO} = 60 pF		2.2		
		V_{SO_STEP} = 1.5 V, G_{CSA} = 40 V/V C_{SO} = 60 pF		2.2		
		V_{SO_STEP} = 1.5 V, G_{CSA} = 80 V/V C_{SO} = 60 pF		3		

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4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BLK, SPI}$	Sense amplifier output blanking time SPI Device	CSA_BLK = 000b, % of t_{DRIVE} period		0		%
		CSA_BLK = 001b, % of t_{DRIVE} period		25		
		CSA_BLK = 010b, % of t_{DRIVE} period		37.5		
		CSA_BLK = 011b, % of t_{DRIVE} period		50		
		CSA_BLK = 100b, % of t_{DRIVE} period		62.5		
		CSA_BLK = 101b, % of t_{DRIVE} period		75		
		CSA_BLK = 110b, % of t_{DRIVE} period		87.5		
		CSA_BLK = 111b, % of t_{DRIVE} period		100		
$t_{BLK, H/W}$	Sense amplifier output blanking time H/W Device			0		ns
t_{SLEW}	Output slew rate	C_{SO} = 60 pF		2.5		V/µs
$V_{BIAS, SPI}$	Output voltage bias SPI Device	V_{SPx} = V_{SNx} = 0 V, CSA_DIV = 0b		V_{AREF} / 2		V
		V_{SPx} = V_{SNx} = 0 V, CSA_DIV = 1b		V_{AREF} / 8		
$V_{BIAS, H/W}$	Output voltage bias H/W Device			V_{AREF} / 2		V
V_{LINEAR}	Linear output voltage range	V_{AREF} = 3.3 V = 5 V	0.25		V_{AREF} – 0.25	V
V_{OFF}	Input offset voltage	V_{SPx} = V_{SNx} = 0 V, T_J = 25°C	–1		1	mV
V_{OFF_D}	Input offset voltage drift	V_{SPx} = V_{SNx} = 0 V		±10	±25	µV/°C
I_{BIAS}	Input bias current	V_{SPx} = V_{SNx} = 0 V			100	µA
I_{BIAS_OFF}	Input bias current offset	I_{SPx} – I_{SNx}	–1		1	µA
I_{AREF}	AREF input current	V_{VREF} = 3.3 V = 5 V DRV8718-Q1 RVJ, DRV8714-Q1 RVJ		2	3	mA
CMRR	Common mode rejection ratio	DC, –40 ≤ T_J ≤ 125°C	72	90		dB
		DC, –40 ≤ T_J ≤ 150°C	69	90		
		20kHz		80		
PSRR	Power supply rejection ratio	PVDD to SOx, DC		100		dB
		PVDD to SOx, 20kHz		90		
		PVDD to SOx, 400kHz		70		
PROTECTION CIRCUITS						
V_{PVDD_UV}	PVDD undervoltage threshold	V_{PVDD} rising	4.325	4.625	4.9	V
		V_{PVDD} falling	4.25	4.525	4.8	
$V_{PVDD_UV_HYS}$	PVDD undervoltage hysteresis	Rising to falling threshold		100		mV
$t_{PVDD_UV_DG}$	PVDD undervoltage deglitch time		8	10	12.75	µs
V_{PVDD_OV}	PVDD overvoltage threshold	V_{PVDD} rising, PVDD_OV_LVL = 0b	21	22.5	24	V
		V_{PVDD} falling, PVDD_OV_LVL = 0b	20	21.5	23	
		V_{PVDD} falling, PVDD_OV_LVL = 0b, DRV8714-Q1	19.75	21.5	23	
		V_{PVDD} rising, PVDD_OV_LVL = 1b	27	28.5	30	
		V_{PVDD} falling, PVDD_OV_LVL = 1b	26	27.5	29	
		V_{PVDD} falling, PVDD_OV_LVL = 1b, DRV8714-Q1	25.4	27.5	29	
$V_{PVDD_OV_HYS}$	PVDD overvoltage hysteresis	Rising to falling threshold		1		V

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4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PVDD_OV_DG}$	PVDD overvoltage deglitch time	PVDD_OV_DG = 00b	0.75	1	1.5	µs
		PVDD_OV_DG = 01b	1.5	2	2.5	
		PVDD_OV_DG = 10b	3.25	4	4.75	
		PVDD_OV_DG = 11b	7	8	9	
V_{DVDD_POR}	DVDD supply POR threshold	DVDD falling	2.5	2.7	2.9	V
		DVDD rising	2.6	2.8	3	
$V_{DVDD_POR_HYS}$	DVDD POR hysteresis	Rising to falling threshold		100		mV
$t_{DVDD_POR_DG}$	DVDD POR deglitch time		5	8	12.75	µs
$V_{CP_UV, SPI}$	Charge pump undervoltage threshold SPI Device	V_{VCP} - V_{PVDD}, V_{VCP} falling VCP_UV = 0b	4	4.75	5.5	V
		V_{VCP} - V_{PVDD}, V_{VCP} falling VCP_UV = 1b	5.5	6.25	7	
$V_{CP_UV, H/W}$	Charge pump undervoltage threshold H/W Device		4	4.75	5.5	V
$t_{CP_UV_DG}$	Charge pump undervoltage deglitch time		8	10	12.75	µs
V_{CP_SO}	Charge pump tripler to doubler switch over threshold	V_{PVDD} rising	18	18.75	19.5	V
V_{CP_SO}	Charge pump tripler to doubler switch over threshold	V_{PVDD} falling	17	17.75	18.5	V
$t_{CP_SO_HYS}$	Charge pump tripler to doubler switch over hysteresis			1		V
$t_{CP_SO_DG}$	Charge pump tripler to doubler switch over threshold deglitch		8	10	12.75	µs
V_{GS_CLP}	High-side driver V_{GS} protection clamp		12.5	15	17	V
V_{GS_LVL}	Gate voltage monitor threshold SPI Device	V_{GHx} – V_{SHx}, V_{GLx} – V_{PGNDx} VGS_LVL = 0b	1.1	1.4	1.75	V
		V_{GHx} – V_{SHx}, V_{GLx} – V_{PGNDx} VGS_LVL = 1b	0.75	1	1.2	V
	Gate voltage monitor threshold H/W Device	V_{GHx} – V_{SHx}, V_{GLx} – V_{PGNDx}	1.1	1.4	1.75	V
$t_{GS_FLT_DG}$	V_{GS} fault monitor deglitch time		1.5	2	2.75	µs
$t_{GS_HS_DG}$	V_{GS} handskahe monitor deglitch time			210		ns
$t_{DRIVE, SPI}$	V_{GS} and V_{DS} monitor blanking time SPI Device	VGS_TDRV = 000b	1.5	2	2.5	µs
		VGS_TDRV = 001b	3.25	4	4.75	
		VGS_TDRV = 010b	7.5	8	9	
		VGS_TDRV = 011b	10	12	14	
		VGS_TDRV = 100b	14	16	18	
		VGS_TDRV = 101b	20	24	28	
		VGS_TDRV = 110b	28	32	36	
		VGS_TDRV = 111b	80	96	120	
$t_{DRIVE, H/W}$	V_{GS} and V_{DS} monitor blanking time H/W Device		7.5	8	9	µs

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4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DS_LVL, SPI}$	V_{DS} overcurrent protection threshold SPI Device	VDS_LVL = 0000b	0.04	0.06	0.08	V
		VDS_LVL = 0001b	0.06	0.08	0.10	
		VDS_LVL = 0010b	0.075	0.10	0.125	
		VDS_LVL = 0011b	0.095	0.12	0.145	
		VDS_LVL = 0100b	0.11	0.14	0.17	
		VDS_LVL = 0101b	0.13	0.16	0.19	
		VDS_LVL = 0110b	0.15	0.18	0.21	
		VDS_LVL = 0111b	0.17	0.2	0.23	
		VDS_LVL = 1000b	0.255	0.3	0.345	
		VDS_LVL = 1001b	0.35	0.4	0.45	
		VDS_LVL = 1010b	0.44	0.5	0.56	
		VDS_LVL = 1011b	0.52	0.6	0.68	
		VDS_LVL = 1100b	0.61	0.7	0.79	
		VDS_LVL = 1101b	0.88	1	1.12	
		VDS_LVL = 1110b	1.2	1.4	1.6	
		VDS_LVL = 1111b	1.75	2	2.25	
$V_{DS_LVL, H/W}$	V_{DS} overcurrent protection threshold H/W Device	VDS six-level input 1	0.04	0.06	0.08	V
		VDS six-level input 2	0.075	0.10	0.125	
		VDS six-level input 3	0.17	0.2	0.23	
		VDS six-level input 4	0.44	0.5	0.56	
		VDS six-level input 5	0.88	1	1.12	
		VDS six-level input 6		Disabled		
$t_{DS_DG, SPI}$	V_{DS} overcurrent protection deglitch time SPI Device	VDS_DG = 00b(1)	0.75	1	1.5	µs
		VDS_DG = 01b	1.5	2	2.5	
		VDS_DG = 10b	3.25	4	4.75	
		VDS_DG = 11b	7.5	8	9	
$t_{DS_DG, H/W}$	V_{DS} overcurrent protection deglitch time H/W Device		3.25	4	4.75	µs
I_{OLD}	Offline diagnostic current source	Pull up current		3		mA
		Pull down current		3		
R_{OLD}	Offline open load resistance detection threshold	VDS_LVL = 1.4 V, 4.9 V ≤ V_{DRAIN} ≤ 18 V		22	50	kΩ
		VDS_LVL = 1.4 V, 4.9 V ≤ V_{DRAIN} ≤ 37 V		22	105	kΩ
		VDS_LVL = 2 V, 4.9 V ≤ V_{DRAIN} ≤ 18 V		10	25	kΩ
		VDS_LVL = 2 V, 4.9 V ≤ V_{DRAIN} ≤ 37 V		10	50	kΩ
t_{WD}	Watchdog timer period	WD_WIN = 0b	36	40	44	ms
		WD_WIN = 1b	90	100	110	
V_{POB_OV}	Power off braking overvoltage threshold	Rising	28	30.5	33	V
		Falling	25	27	29.5	V
$V_{POB_OV_HYS}$	Power off braking overvoltage hysteresis			3		V
I_{POB_P}	Power off braking gate source current			15		mA
I_{POB_N}	Power off braking gate sink current			27		mA
V_{POB}	Power off braking gate pull up voltage	V_{PVDD} ≥ 8V	5.5		12.5	V

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4.9 V ≤ V_{PVDD} ≤ 37 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for V_{PVDD} = 13.5 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{POB_ON}	Power off braking turn-on time			13		µs
t_{POB_OFF}	Power off braking turn-off time			2.5		µs
V_{POB_VDS}	Power off braking VDS comparator threshold	Rising, DRV8714-Q1, DRV8718-Q1	250	350	450	mV
		Rising, DRV8714A-Q1	600	800	1000	mV
t_{POB_VDS}	Power off braking VDS comparator deglitch		2.5	4	5.75	µs
T_{OTW}	Thermal warning temperature	T_J rising	130	150	170	°C
T_{HYS}	Thermal warning hysteresis			20		°C
T_{OTSD}	Thermal shutdown temperature	T_J rising	150	170	190	°C
T_{HYS}	Thermal shutdown hysteresis			20		°C

(1) t_{DS_DG} 1µs (VDS_DG = 00b) should not be utilized for V_{DS_LVL} 0.06, 0.08, and 0.10 V (VDS_LVL = 0000b, 0001b, 0010b)

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{H_SDI}	SDI input data hold time	25			ns
t_{D_SDO}	SDO output data delay time, C_L = 20 pF			30	ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{H_nSCS}	nSCS input hold time	25			ns
t_{HI_nSCS}	nSCS minimum high time	450			ns
t_{EN_nSCS}	Enable delay time, nSCS low to SDO active			50	ns
t_{DIS_nSCS}	Disable delay time, nSCS high to SDO hi-Z			50	ns

6.7 Timing Diagrams

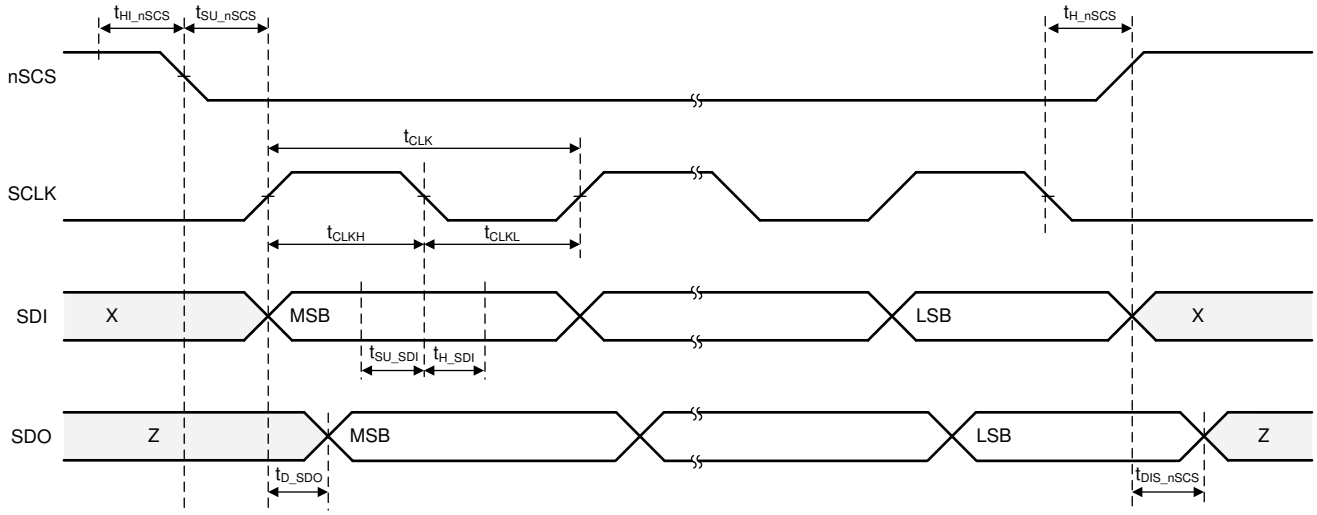

Figure 6-1. SPI Timing Diagram

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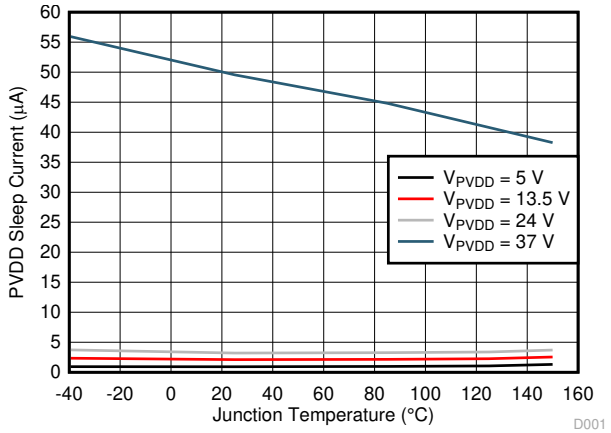
6.8 Typical Characteristics



V_{PVDD} = 37 V, additional leakage to V_{POB_OV} comparator.

Figure 6-2. PVDD Sleep Current

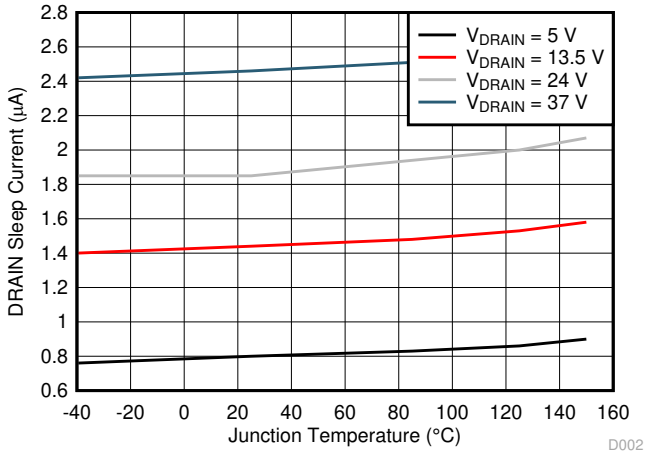


Figure 6-3. DRAIN Sleep Current

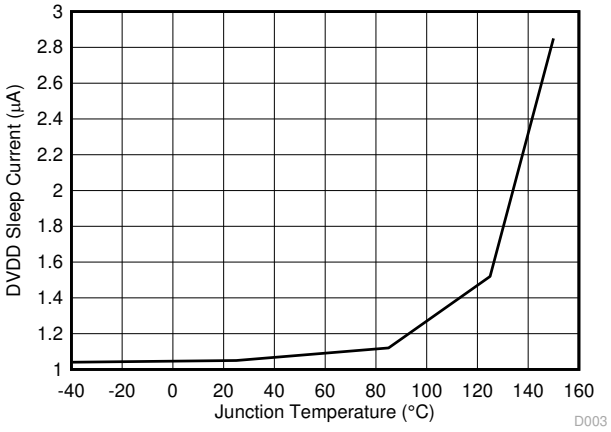


Figure 6-4. DVDD Sleep Current

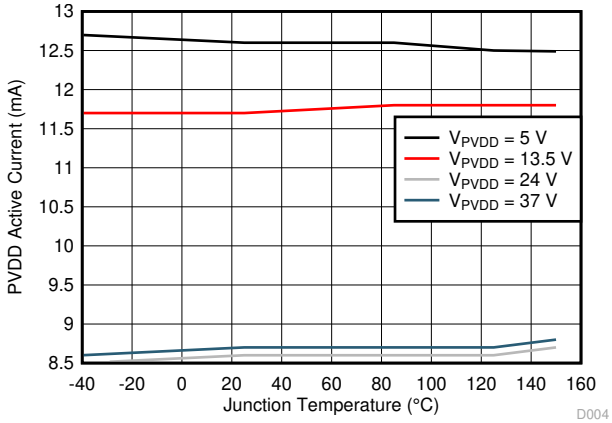


Figure 6-5. PVDD Active Current

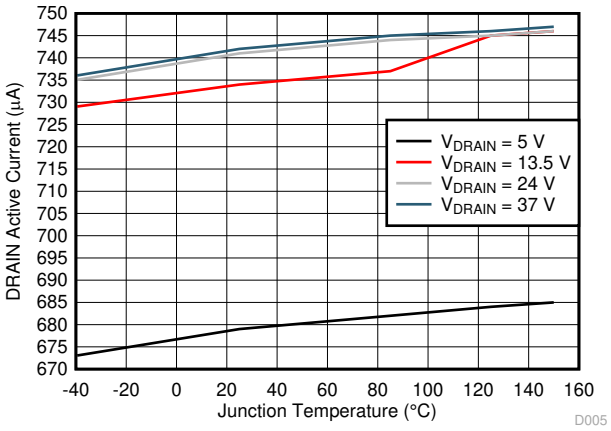


Figure 6-6. DRAIN Active Current

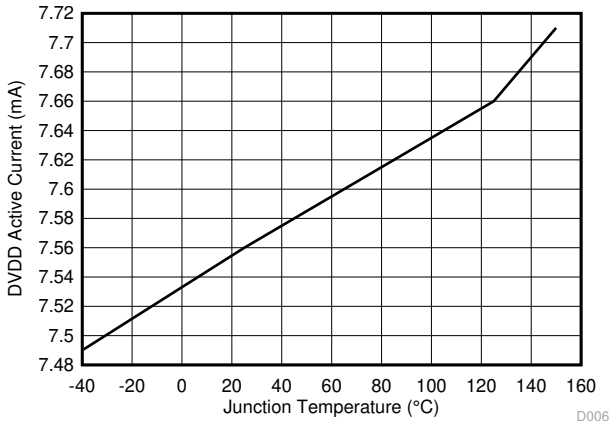
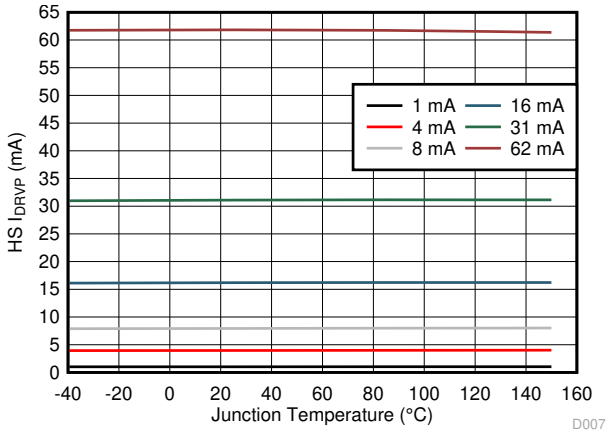
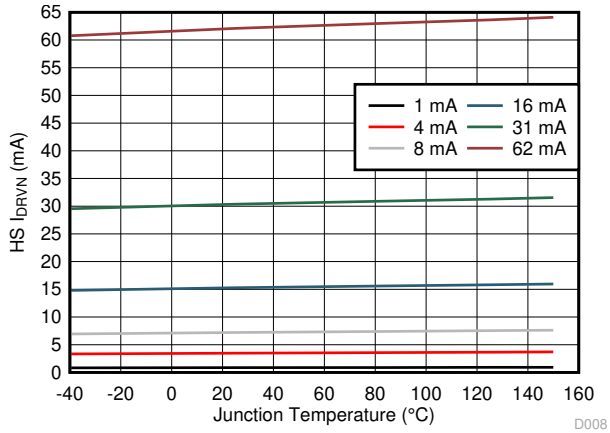


Figure 6-7. DVDD Active Current



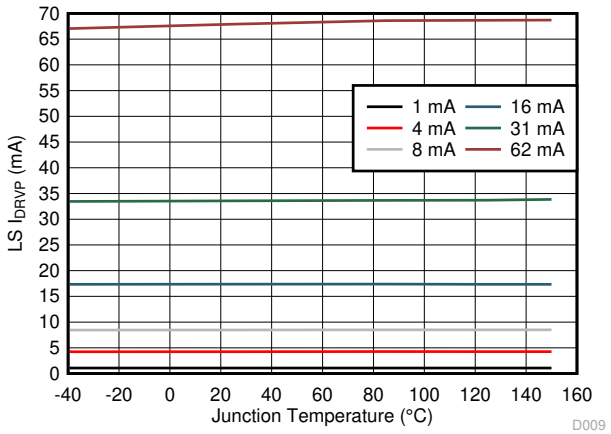
V_{PVDD} = 13.5 V

Figure 6-8. High-Side Gate Driver Source Current



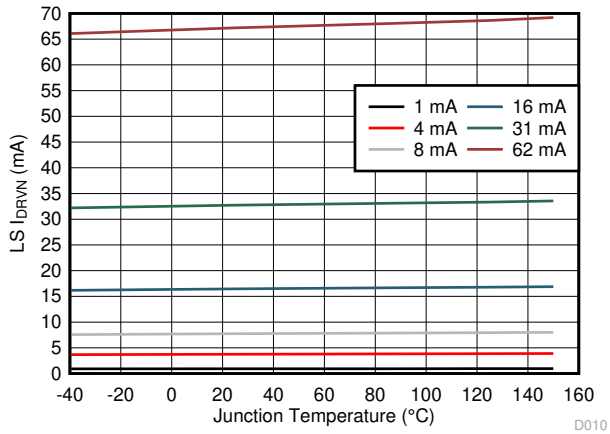
V_{PVDD} = 13.5 V

Figure 6-9. High-Side Gate Driver Sink Current



V_{PVDD} = 13.5 V

Figure 6-10. Low-Side Gate Driver Source Current



V_{PVDD} = 13.5 V

Figure 6-11. Low-Side Gate Driver Sink Current

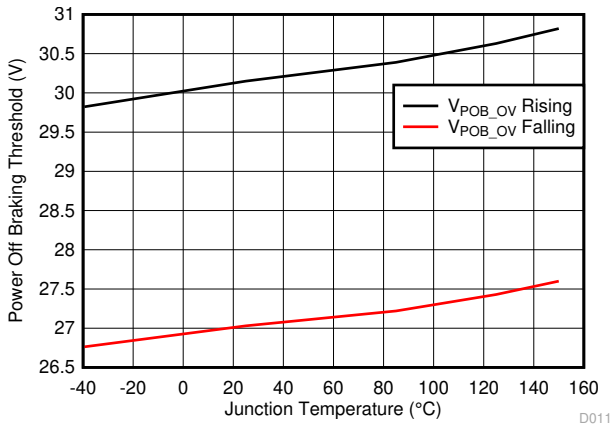


Figure 6-12. Power Off Braking Threshold

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7 Detailed Description

7.1 Overview

The DRV871x-Q1 family of devices are highly integrated, multi-channel gate drivers intended for driving multiple motors or loads in automotive applications. The devices are tailored for automotive applications by providing a wide array of configuration and control options, MOSFET slew control, MOSFET propagation delay control, and advanced diagnostic and protection functions. The devices provide either 4 (DRV8714-Q1) or 8 (DRV8718-Q1) half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV871x-Q1 family of devices reduce total system cost by integrating a high number of gate drivers, driver power supples, current shunt amplifiers, and protection monitors.

The DRV871x-Q1 family of devices support a wide array of input PWM control modes. These range from half-bridge control, H-bridge control, and grouped H-bridge control through PWM multiplexing. Recirculation and muxing schemes can be configured through the device SPI interface and input pins. This allows for the device to support different configurations of the outputs such as individual or grouped multiple motor control schemes.

The DRV871x-Q1 devices are based on a smart gate drive architecture (SGD) to reduce system cost and improve reliability. The SGD architecture optimizes dead time to avoid shoot-through conditions, provides flexibility in decreasing electromagnetic interference (EMI) with MOSFET slew rate control through adjustable gate drive current, improves MOSFET propagation delay and matching with an adaptive controller, and protects against drain to source and gate short circuits conditions with V_{DS} and V_{GS} monitors. A strong pulldown circuit helps prevent dV/dt parasitic gate coupling. The external MOSFET slew control is supported through adjustable output gate drivers. The gate driver peak source and sink current can be configured between 0.5-mA and 62-mA with an additional low current mode to achieve gate drive source and sink currents less than 0.5-mA.

The devices can operate with either 3.3-V or 5-V external controllers (MCUs). A dedicated DVDD pins allows for external power to the device digital core and the digital outputs to be referenced to the controller I/O voltage. It communicates with the external controller through an SPI bus to manage configuration settings and diagnostic feedback. The device also has an AREF pin which allows for the shunt amplifier reference voltage to be connected to the reference voltage of the external controller ADC. The shunt amplifier outputs are also clamped to the AREF pin voltage to protect the inputs of the controller from excessive voltage spikes.

The devices provides an array of diagnostic and protection features to monitor system status before operation and protect against faults during system operation. These include under and overvoltage monitors for the power supply and charge pump, V_{DS} overcurrent and V_{GS} gate fault monitors for the external MOSFETs, offline open load and short circuit detection, windowed watchdog timer for SPI and MCI diagnostics, and internal thermal warning and shutdown protection. The current shunt amplifier can be utilized to monitor load current of the system. The high common mode range of the amplifier allows for either inline, high-side, or low-side based shunt resistor current sensing.

Lastly, the device has a unique power off braking function that gives the ability to enables the low-side drivers during the device's low-power sleep mode in case of detecting a system overvoltage condition. This can be utilized to prevent motor back-emf from overcharging the system voltage rail.

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7.2 Functional Block Diagram

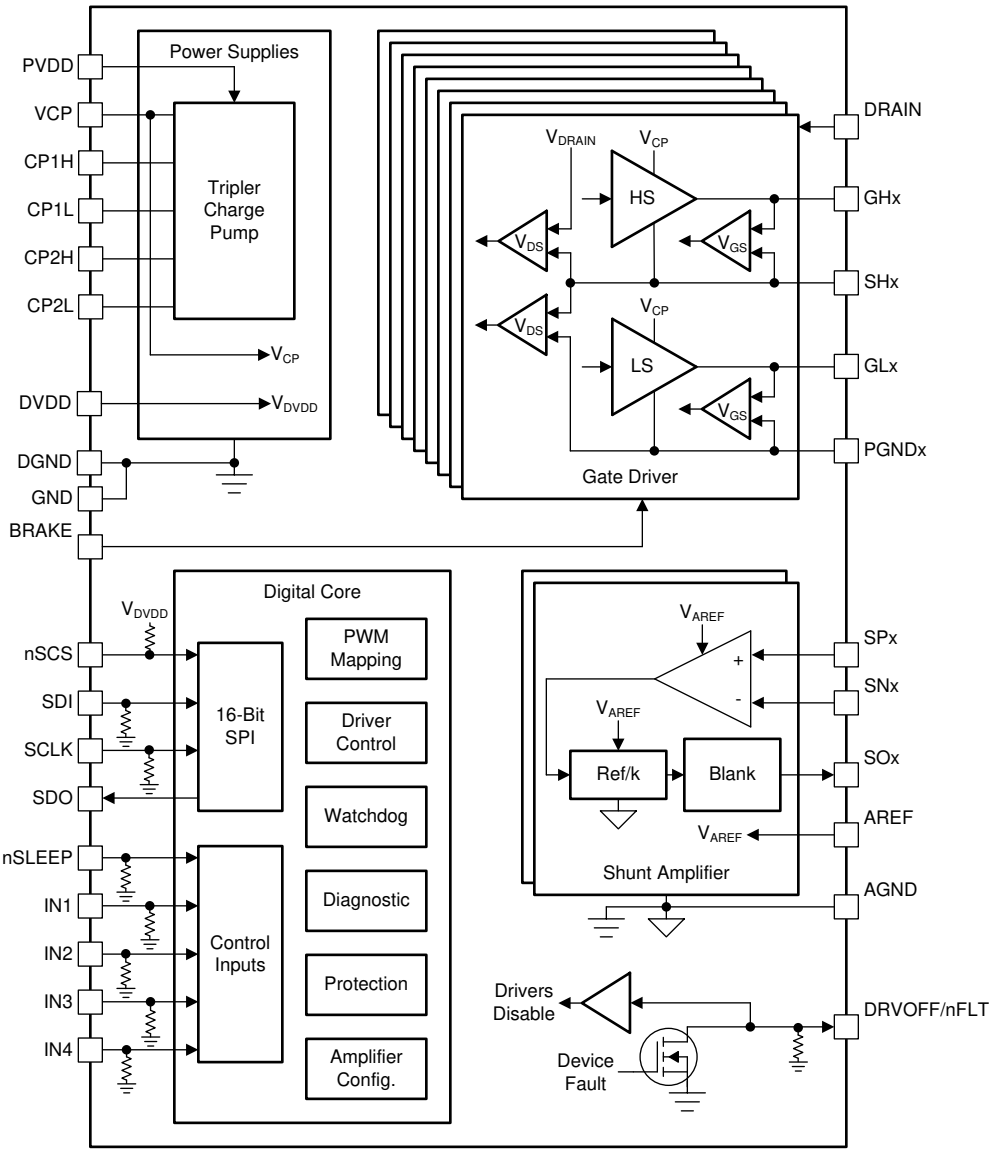

Figure 7-1. Block Diagram for DRV8718S-Q1 RVJ Package

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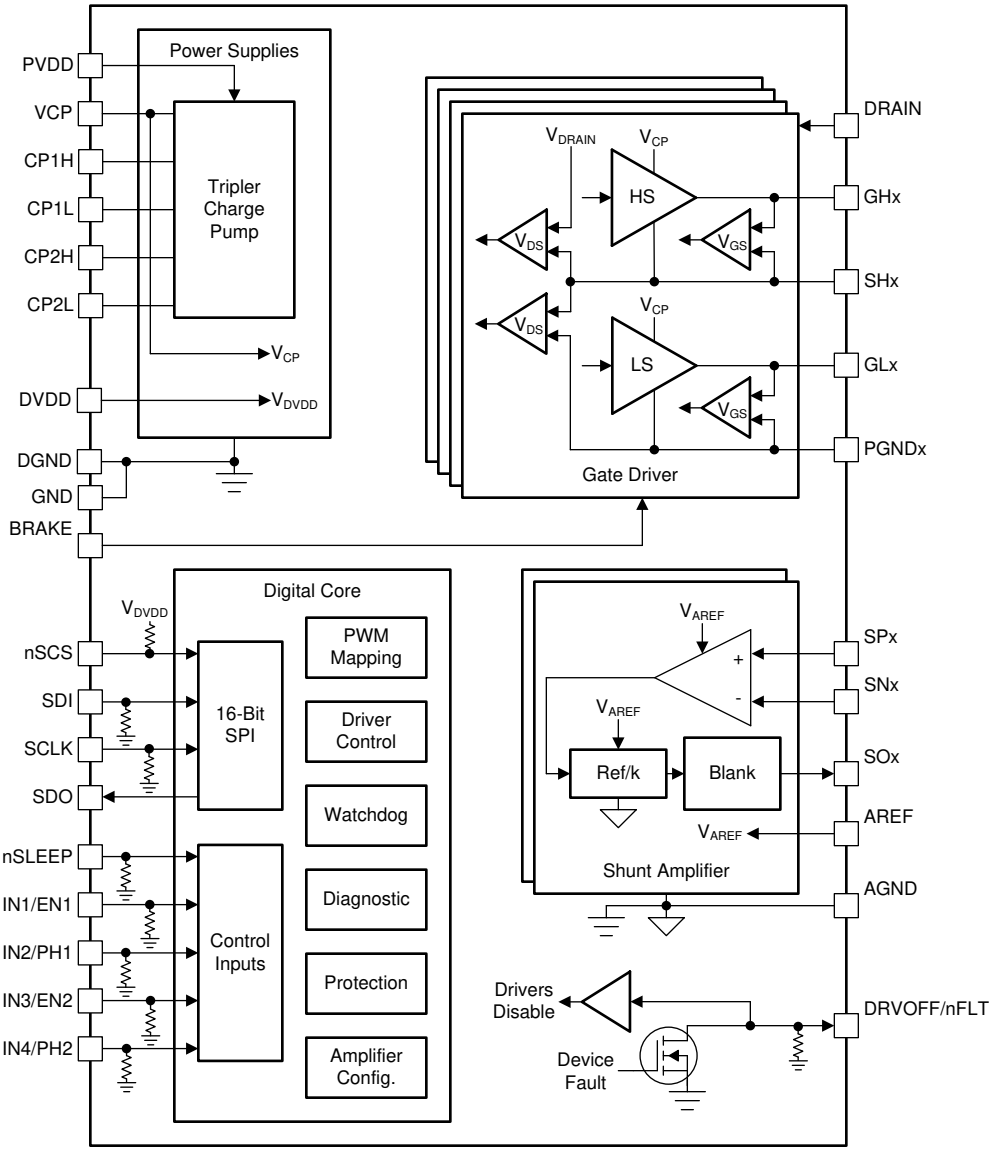

Figure 7-2. Block Diagram for DRV8714S-Q1 RVJ Package

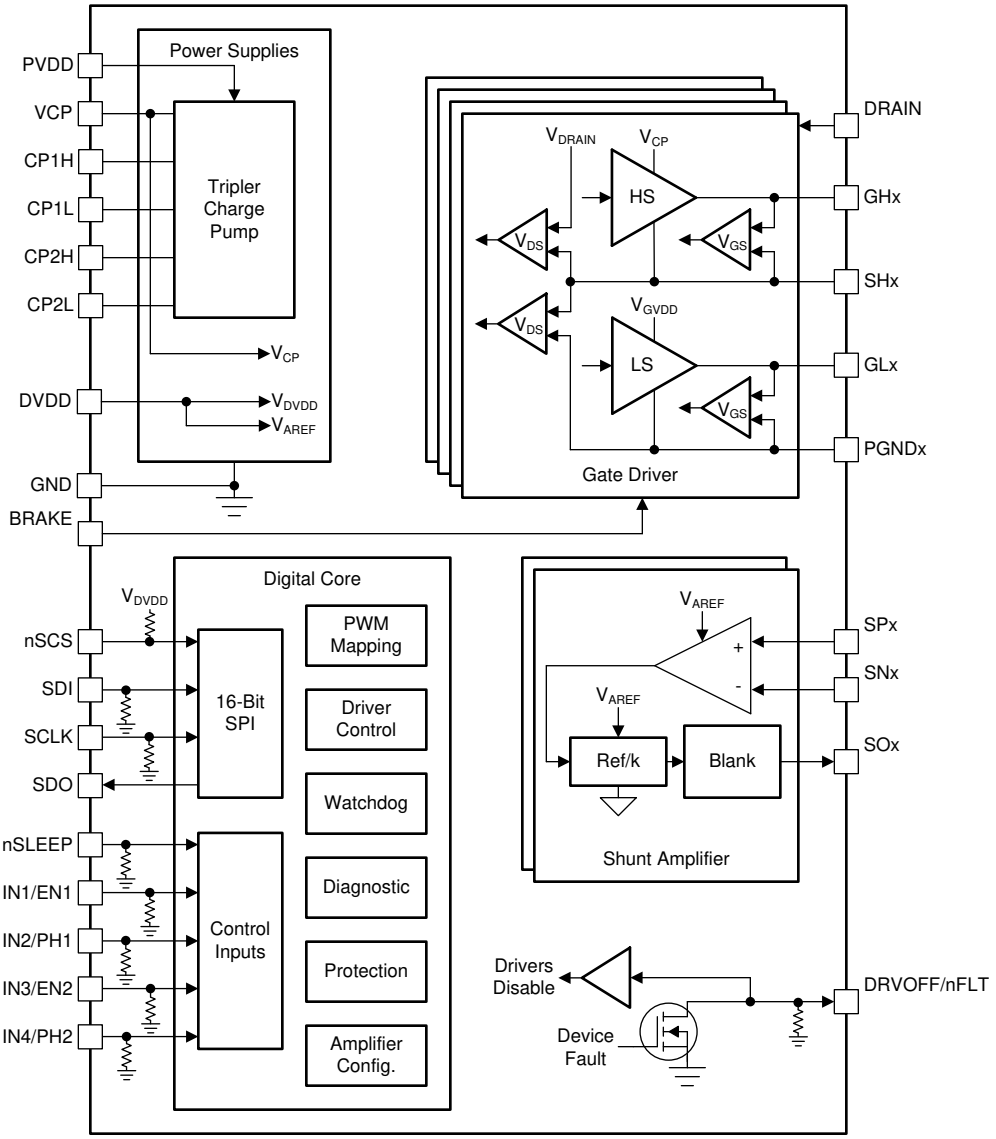

Figure 7-3. Block Diagram for DRV8714S-Q1 RHA Package

Note

On the DRV8714-Q1 RHA package, the AREF pin is not present. The AREF power supply is derived from the DVDD pin.

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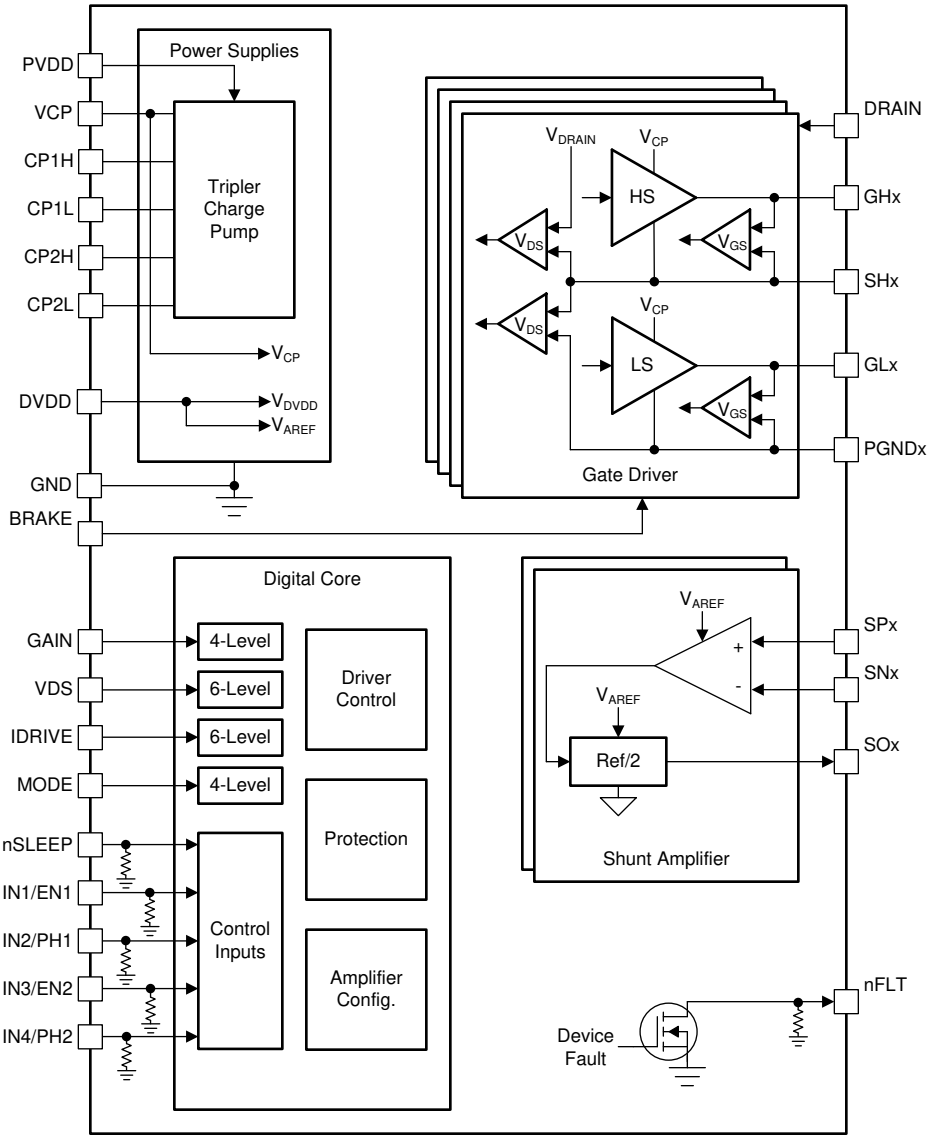

Figure 7-4. Block Diagram for DRV8714H-Q1 RHA Package

Note

On the DRV8714-Q1 RHA package, the AREF pin is not present. The AREF power supply is derived from the DVDD pin.

7.3 Feature Description

7.3.1 External Components

Table 7-1 lists the recommended external components for the device.

Table 7-1. Recommended External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{PVDD1}	PVDD	GND	0.1-µF, low ESR ceramic capacitor, PVDD-rated.
C_{PVDD2}	PVDD	GND	Local bulk capacitance greater than or equal to 10-µF, PVDD-rated.
C_{DVDD} (1)	DVDD	GND	1.0-µF, 6.3-V, low ESR ceramic capacitor
C_{AREF} (1)	AREF(3)	GND	0.1-µF, 6.3-V, low ESR ceramic capacitor
C_{VCP}	VCP	PVDD	1-µF 16-V, low ESR ceramic capacitor
C_{FLY1}	CP1H	CP1L	0.1-µF, PVDD-rated, low ESR ceramic capacitor
C_{FLY2}	CP2H	CP2L	0.1-µF, PVDD + 16-V, low ESR ceramic capacitor
R_{nFLT}	VCC(2)	nFLT	Pullup resistor, I_{OD} ≤ 5-mA

(1) A local bypass capacitor is recommended to reduce noise on the external low voltage power supply. If another bypass capacitor is within close proximity of the device for the external low voltage power supply and noise on the power supply is minimal, it is optional to remove this component.
(2) VCC is not a pin on the device, but the external low voltage power supply.
(3) On the DRV8714-Q1 RHA package, the AREF pin is not present and the AREF power supply is derived from the DVDD pin.

7.3.2 Device Interface Variants

The DRV8714-Q1 devices support two different interface modes (SPI and hardware) to allow the end application to design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin to pin compatible. This allows for application designers to evaluate with one interface version and potentially switch to another with minimal modifications to their design. The DRV8718-Q1 device is only available with the SPI interface.

7.3.2.1 Serial Peripheral Interface (SPI)

The DRV8718-Q1 and DRV8714S-Q1 SPI device variants support a serial communication bus that allows for an external controller to send and receive serial data with the driver. This allows for the external controller to configure device settings and read detailed fault information. The interface is a four wire serial interface utilizing the SCLK, SDI, SDO, and nSCS pins.

- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication.
- The SCLK pin is an input which accepts a clock signal to determine when data is captured and propagated on SDI and SDO.
- The SDI pin is the data input
- The SDO pin is the data output. The SDO pin uses a push-pull output structure referenced to the DVDD input.

For more information on the SPI, see the SPI Interface section

7.3.2.2 Hardware (H/W)

The DRV8714H-Q1 hardware interface device variant converts the four SPI pins into four resistor configurable inputs, GAIN, VDS, IDRIVE, and MODE. This allows for the application designer to configure the most commonly used device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

The hardware interface settings are latched on power up of the device. They can reconfigured by putting the device in sleep mode with the nSLEEP pin, changing the setting, and reenabling the device through nSLEEP.

- The GAIN pin configures the current shunt amplifier gain

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- The VDS pin configures the voltage threshold of the V_{DS} overcurrent monitors.
- The IDRIVE pin configures the gate drive current strength.
- The MODE pin configures the PWM input control mode.

For more information on the hardware interface, see the Pin Diagrams section.

7.3.3 Input PWM Control Modes

The DRV8718-Q1 and DRV8714-Q1 support a highly configurable Half-Bridge Control Scheme in order to be adapted for a wide variety of output load configurations and control regulations. This control scheme helps to reduce the number of required PWM channels and pins from the external controller. 4 independent PWM control inputs can be provided to the INx input pins and assigned to any of the output half-bridge drivers. The device internally handles the dead-time generation between high-side and low-side switching so that a single PWM input can be used to control a half-bridge.

Additionally the DRV8714-Q1 supports several other standard control schemes for either H-bridge or solenoid control. These control schemes can be selected through the BRG_MODE register setting on SPI interface devices or MODE pin on H/W interface devices as shown in Table 7-2

Table 7-2. DRV8714-Q1 Input PWM Modes

PWM Mode	SPI Interface (BRG_MODE)	H/W Interface (MODE Pin)
Half-Bridge Control	00b	Level 1 - GND
H-Bridge Control	01b (PH/EN)	Level 2 (PH/EN) - 47k kΩ
	10b (PWM)	Level 3 (PWM) - Hi-Z
Split HS and LS Control	11b	Level 4 - DVDD

7.3.3.1 Half-Bridge Control Scheme With Input PWM Mapping

7.3.3.1.1 DRV8718-Q1 Half-Bridge Control

The DRV8718-Q1 controls the eight half-bridge gate drivers through a combination of direct PWM, PWM multiplexers, and SPI control registers. The HBx_CTRL (half-bridge control) SPI register is used to control the half-bridge gate driver output state. The different control states for the gate drivers are shown in Table 7-3. Any unused half-bridge drivers should be left disconnected and in the high-impedance (Hi-Z) output state.

The DRV8718-Q1 PWM inputs pins (IN1, IN2. IN3, IN4) can be used to set the PWM frequency and duty cycle for the assigned outputs. If higher frequency or precise duty cycle PWM control is not required, the eight half-bridge gate drivers can also be controlled directly through the HBx_CTRL SPI control register.

The DRV8718-Q1 can also be used to control individual high-side or low-side external MOSFETs instead of a half-bridge. In this setup, simply leave the unused GHx/GLx driver of the half-bridge disconnected. Only passive freewheeling should be utilized if PWM control is needed in this setup.

Table 7-3. Half-Bridge SPI Register Control (HBx_CTRL)

HBx_CTRL (1-8)	Gate Driver State	GHx (1-8)	GLx (1-8)	SHx (1-8)
00b	High Impedance (Hi-Z)	L	L	Hi-Z
01b	Drive Low-Side (L)	L	H	L
10b	Drive High-Side (H)	H	L	H
11b	Drive PWM (PWM)	Table 7-5	Table 7-5	Table 7-5

In PWM control mode, the half-bridge gate drivers can be controlled directly by any of 4 independent PWM control inputs (IN1, IN2, IN3, IN4) as shown in Table 7-4.

PWM mapping helps reduce the number of required PWM resources and pins from the external controller when utilizing motor groups or zone control schemes while still allowing for fine PWM frequency and duty cycle control. Each PWM input pin can be mapped to as many half-bridge drivers as desired. The input PWM signal can actively drive the high-side or low-side MOSFET of the half-bridge (based on PWMx_HL control register), with

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the opposite MOSFET in the half-bridge being controlled accordingly based on the freewheeling setting. Either active or passive freewheeling can be configured by the PWMx_FW control register.

The following steps should be taken to modify the PWM mapping scheme during driver operation.

- Set active half-bridge to Hi-Z mode through HBx_CTRL.
- Set new target half-bridge to Hi-Z mode through HBx_CTRL.
- HBx_PWM mapping should be updated from the old target to the new target half-bridge.
- Set new target half-bridge drive MOSFET (PWMx_HL) and freewheeling settings (PWMx_FW).
- Set new target half-bridge to PWM mode through HBx_CTRL.

Table 7-4. Half-Bridge PWM Mapping (HBx_PWM)

PWM Mapping	
HBx_PWM (1-8)	**Input PWM Source**
00b	IN1
01b	IN2
10b	IN3
11b	IN4

Table 7-5. Half-Bridge PWM Control (PWMx_HL and PWMx_FW)

HBx_PWM (1-8)	HBx_HL (1-8)	HBx_FW (1-8)	Gate Driver State	GHx (1-8)	GLx (1-8)	SHx (1-8)
PWMx	0	0	PWM High-Side Active FW	PWMx	!PWMx	PWMx
	1		PWM Low-Side Active FW	!PWMx	PWMx	!PWMx
	0	1	PWM High-Side Passive FW	PWMx	L	PWMx
	1		PWM Low-Side Passive FW	L	PWMx	!PWMx

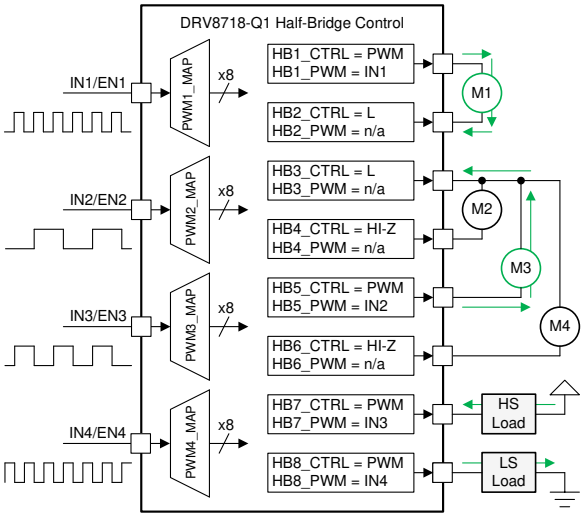

Figure 7-5. PWM Mapping Example 1

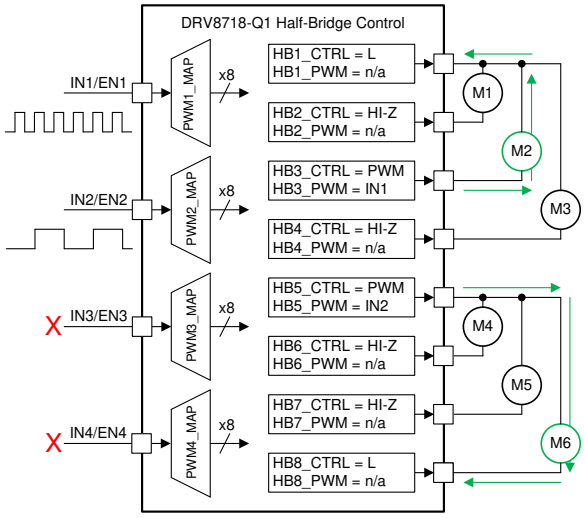

Figure 7-6. PWM Mapping Example 2

7.3.3.1.2 DRV8714-Q1 Half-Bridge Control

The DRV8714-Q1 controls the four half-bridge gate drivers through a combination of direct PWM, PWM multiplexers, and SPI control registers. The half-bridge control mode can be enabled by setting BRG_MODE = 00b on SPI interface variants or the MODE pin to level 1 on H/W interface variants. On SPI interface variants,

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the HBx_CTRL (half-bridge control) SPI register is used to control the half-bridge gate driver output state. The different control states for the gate drivers are shown in Table 7-6. Any unused half-bridge drivers should be left disconnected and in the high-impedance (Hi-Z) output state. On H/W interface variants, the device defaults to direct PWM control from the associated INx/ENx input pins.

The DRV8714-Q1 PWM inputs pins (IN1/EN1, IN2/PH1. IN3/EN2, IN4/PH2) can be used to set the PWM frequency and duty cycle for the assigned output. If high frequency or precise duty cycle PWM control is not required, the four half-bridge gate drivers can be controlled directly through the HBx_CTRL SPI control register on SPI interface variants.

The DRV8714-Q1 can also be used to control individual high-side or low-side external MOSFETs instead of a half-bridge. In this setup, simply leave the unused GHx/GLx driver of the half-bridge disconnected. Only passive freewheeling should be utilized if PWM control is needed in this setup.

Table 7-6. Half-Bridge SPI Register Control (HBx_CTRL)

HBx_CTRL (1-4)	Gate Driver State	GHx (1-4)	GLx (1-4)	SHx (1-4)
00b	High Impedance (Hi-Z)	L	L	Hi-Z
01b	Drive Low-Side (L)	L	H	L
10b	Drive High-Side (H)	H	L	H
11b	Drive PWM (PWM)	Table 7-8	Table 7-8	Table 7-8

In PWM control mode, the half-bridge gate drivers can be controlled directly by any of 4 independent PWM control inputs (IN1, IN2, IN3, IN4) as shown in Table 7-4. On H/W interface variants, the PWM control inputs map directly to their associated output number.

PWM mapping helps reduce the number of required PWM resources and pins from the external controller when utilizing motor groups or zone control schemes while still allowing for fine PWM frequency and duty cycle control. Each PWM input pin can be mapped to as many half-bridge drivers as desired. The input PWM signal can actively drive the high-side or low-side MOSFET of the half-bridge (based on PWMx_HL control register), with the opposite MOSFET in the half-bridge being controlled accordingly based on the freewheeling setting. Either active or passive freewheeling can be configured by the PWMx_FW control register. On H/W interface variants, the device is configured for high-side PWM drive with active freewheeling.

The following steps should be taken to modify the PWM mapping scheme during driver operation.

- Set active half-bridge to Hi-Z mode through HBx_CTRL.
- Set new target half-bridge to Hi-Z mode through HBx_CTRL.
- HBx_PWM mapping should be updated from the old target to the new target half-bridge.
- Set new target half-bridge drive MOSFET (PWMx_HL) and freewheeling settings (PWMx_FW).
- Set new target half-bridge to PWM mode through HBx_CTRL.

Table 7-7. Half-Bridge PWM Mapping (PWMx_MAP)

PWM Mapping	
HBx_PWM (1-4)	Input PWM Source
00b	IN1
01b	IN2
10b	IN3
11b	IN4

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Table 7-8. Half-Bridge PWM Control (PWMx_HL and PWMx_FW)

HBx_PWM (1-4)	HBx_HL (1-4)	HBx_FW (1-4)	Gate Driver State	GHx (1-4)	GLx (1-4)	SHx (1-4)
PWMx	0	0	PWM High-Side Active FW	PWMx	!PWMx	PWMx
	1		PWM Low-Side Active FW	!PWMx	PWMx	!PWMx
	0	1	PWM High-Side Passive FW	PWMx	L	PWMx
	1		PWM Low-Side Passive FW	L	PWMx	!PWMx

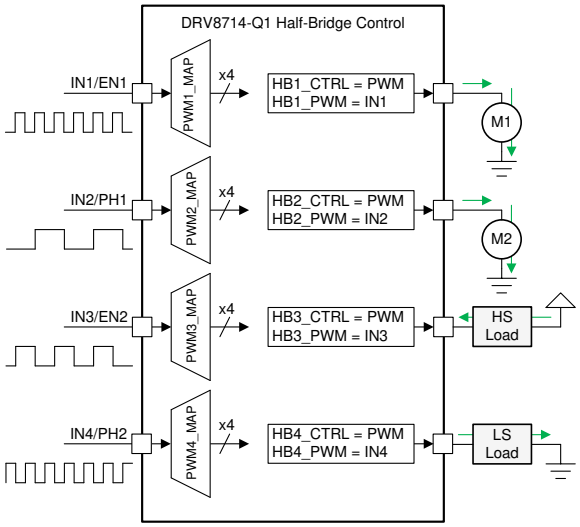

Figure 7-7. PWM Mapping Example 1

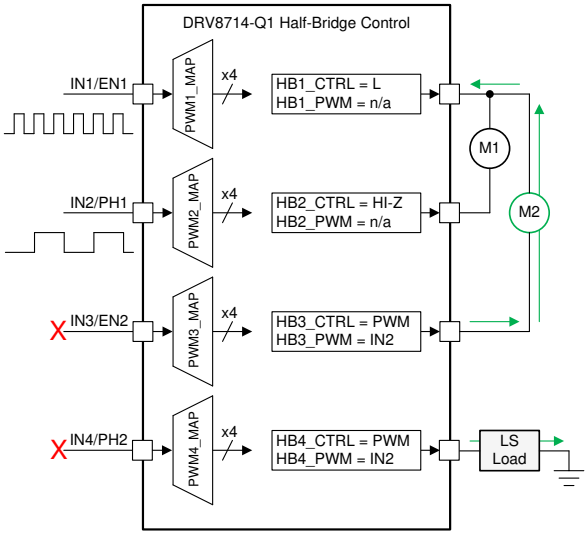

Figure 7-8. PWM Mapping Example 2

7.3.3.2 H-Bridge Control

7.3.3.2.1 DRV8714-Q1 H-Bridge Control

In the H-bridge control mode, each two pairs of half-bridge gate drivers can be controlled as an H-bridge gate driver for a total of two H-bridge gate drivers for the DRV8714-Q1. The H-bridge pairs are half-bridges 1 / 2 and 3 / 4 for the DRV8714-Q1. The DRV8714-Q1 can control the 2 H-bridge gate driver pairs through direct inputs pins or SPI control registers. The H-bridge gate drivers have two input control modes that can be configured through the BRG_MODE register setting (01b = PH/EN and 10b = PWM) on SPI interface variants or the MODE pin (Level 2 = PH/EN and Level 3 = PWM) on H/W interface variants. The PH/EN mode allows for the H-bridge to be controlled with a speed/direction type of interface commanded by one PWM signal and one GPIO signal. The PWM mode allows for the H-bridge to be controlled with a more advanced scheme typically requiring two PWM signals. This allows the H-bridge driver to enter four different output states for additional control flexibility if required.

The DRV8714-Q1 PWM inputs pins (IN1/EN1, IN2/PH1, IN3/EN2, IN4/PH2) are used to set the PWM frequency and duty cycle for the assigned output. If PWM control is not required, the two h-bridge gate drivers can be controlled directly through the SPI control registers. The INx/ENx and INx/PHx SPI control can be enabled through the INx/ENx_MODE and INx/PHx_MODE register settings. Each H-bridge can be individually set to Hi-Z through the HIZ register setting.

The default active freewheeling mode is active low-side. The DRV8714-Q1 SPI interface variants provide the ability to configure the freewheeling state through the FW register setting. This setting can be utilized to modify

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the bridge between low-side or high-side active freewheeling. The H/W interface variants default to low-side freewheeling.

The PH/EN control logic and output states for the gate drivers are shown in Table 7-9 and Table 7-10.

Table 7-9. PH/EN H-Bridge (1 / 2) Control

INPUT				OUTPUT						
IN1/EN1	IN2/PH1	FW1	HIZ1	GH1	GL1	GH2	GL2	SH1	SH2	DESCRIPTION
0	X	0b	0	L	H	L	H	L	L	Low-Side Active Freewheel
0	X	1b	0	H	L	H	L	H	H	High-Side Active Freewheel
1	0	X	0	L	H	H	L	L	H	Drive SH2 → SH1 (Reverse)
1	1	X	0	H	L	L	H	H	L	Drive SH1 → SH2 (Forward)
X	X	X	1	L	L	L	L	HI-Z	HI-Z	High-Impedance

Table 7-10. PH/EN H-Bridge (3 / 4) Control

INPUT				OUTPUT						
IN3/EN2	IN4/PH2	FW2	HIZ2	GH3	GL3	GH4	GL4	SH3	SH4	DESCRIPTION
0	X	0b	0	L	H	L	H	L	L	Low-Side Active Freewheel
0	X	1b	0	H	L	H	L	H	H	High-Side Active Freewheel
1	0	X	0	L	H	H	L	L	H	Drive SH4 → SH3 (Reverse)
1	1	X	0	H	L	L	H	H	L	Drive SH3 → SH4 (Forward)
X	X	X	1	L	L	L	L	HI-Z	HI-Z	High-Impedance

The PWM control logic and output states for the gate drivers are shown in Table 7-11 and Table 7-12

Table 7-11. PWM H-Bridge (1 / 2) Control

INPUT				OUTPUT						
IN1/EN1	IN2/PH1	FW1	HIZ1	GH1	GL1	GH2	GL2	SH1	SH2	DESCRIPTION
0	0	X	0	L	L	L	L	HI-Z	HI-Z	Diode Freewheel (Coast)
0	1	X	0	L	H	H	L	L	H	Drive SH2 → SH1 (Reverse)
1	0	X	0	H	L	L	H	H	L	Drive SH1 → SH2 (Forward)
1	1	0b	0	L	H	L	H	L	L	Low-Side Active Freewheel
1	1	1b	0	H	L	H	L	H	H	High-Side Active Freewheel
X	X	X	1	L	L	L	L	HI-Z	HI-Z	High-Impedance

Table 7-12. PWM H-Bridge (3 / 4) Control

INPUT				OUTPUT						
IN3/EN2	IN4/PH2	FW2	HIZ2	GH3	GL3	GH4	GL4	SH3	SH4	DESCRIPTION
0	0	X	0	L	L	L	L	HI-Z	HI-Z	Diode Freewheel (Coast)
0	1	X	0	L	H	H	L	L	H	Drive SH4 → SH3 (Reverse)
1	0	X	0	H	L	L	H	H	L	Drive SH3 → SH4 (Forward)
1	1	0b	0	L	H	L	H	L	L	Low-Side Active Freewheel
1	1	1b	0	H	L	H	L	H	H	High-Side Active Freewheel
X	X	X	1	L	L	L	L	HI-Z	HI-Z	High-Impedance

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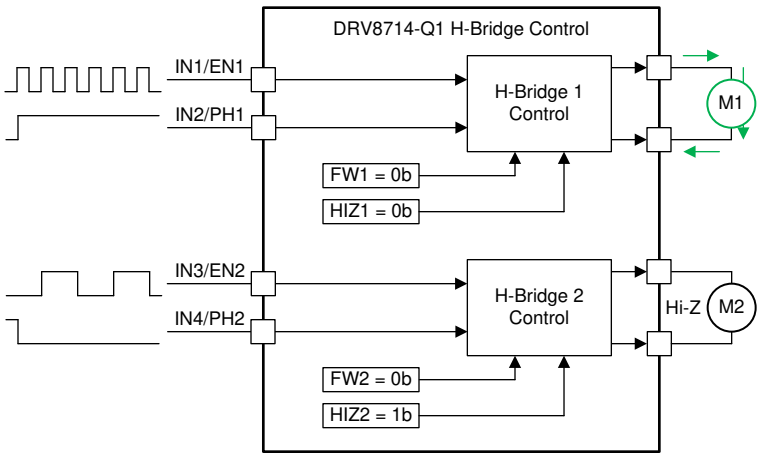

Figure 7-9. H-Bridge Control Example

7.3.3.3 Split HS and LS Solenoid Control

7.3.3.3.1 DRV8714-Q1 Split HS and LS Solenoid Control

In split HS and LS solenoid control mode, the H-bridge pairs (1 / 2 and 3 / 4) are configured to simplify solenoid control schemes as shown in Figure 7-10. This mode allows for the H-bridge to be configured to drive a floating solenoid load between the opposite high-side and low-side external MOSFETs. The solenoid control mode can be enabled by setting the BRG_MODE control register to 11b on SPI interface variants and MODE pin to Level 4 on H/W interface variants..

The high-side MOSFET of the primary half-bridge acts as a HS disconnect switch (controlled through the INx/PHx pin or S_PHx control registers) and the low-side MOSFET of the secondary half-bridge acts as the PWM control for the solenoid (controlled through the INx/ENx pin or S_ENx control register. The INx/ENx and INx/PHx SPI control can be enabled through the INx/ENx_MODE and INx/PHx_MODE register settings. The primary half-bridge low-side MOSFET control is disabled and the secondary half-bridge high-side MOSFET control is disabled. The control truth table is shown in Table 7-13 and Table 7-14.

Table 7-13. Split HS and LS (1 / 2) Control

IN1/EN1	IN2/PH1	GH1	GL1	GH2	GL2	DESCRIPTION
0	X	X	Inactive	Inactive	L	Solenoid PWM Off
1	X	X	Inactive	Inactive	H	Solenoid PWM On
X	0	L	Inactive	Inactive	X	Solenoid Disabled
X	1	H	Inactive	Inactive	X	Solenoid Enabled

Table 7-14. Split HS and LS (3 / 4) Control

IN3/EN2	IN4/PH2	GH3	GL3	GH4	GL4	DESCRIPTION
0	X	X	Inactive	Inactive	L	Solenoid PWM Off
1	X	X	Inactive	Inactive	H	Solenoid PWM On
X	0	L	Inactive	Inactive	X	Solenoid Disabled
X	1	H	Inactive	Inactive	X	Solenoid Enabled

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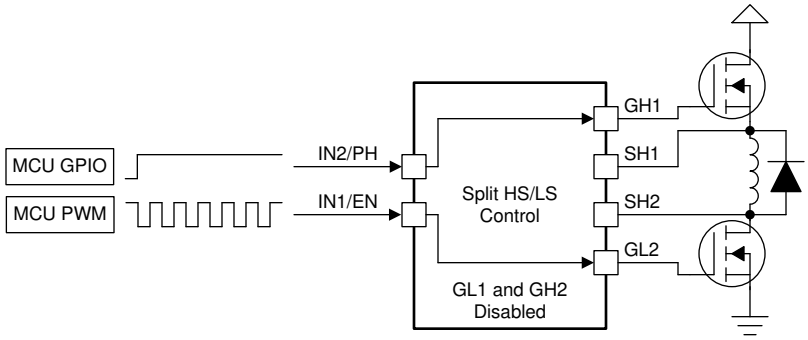

Figure 7-10. Solenoid Control Example

7.3.4 Smart Gate Driver

The DRV871x-Q1 provides an advanced, adjustable floating smart gate driver architecture to provide fine MOSFET control and robust switching performance. The DRV871x-Q1 provides driver functions for slew rate control and a driver state machine for dead-time handshaking, parasitic dV/dt gate coupling prevention, and MOSFET gate fault detection.

Advanced adaptive drive functions are provided for reducing propagation delay, reducing duty cycle distortion, and closed loop programmable slew time. The advanced smart gate driver functions are only available in the Half-Bridge Control PWM mode and on SPI device variants. The advanced functions do not interfere with standard operation of the gate drivers and can be utilized as needed by system requirements.

The different functions of the smart gate drive architecture are summarized below with additional details in the following sections.

Smart Gate Driver Core Functions:

- Gate Driver Functional Block Diagram
- Slew Rate Control (IDRIVE)
- Gate Driver State Machine (TDRIVE)
- Advanced: Propagation Delay Reduction (PDR)
- Advanced: Duty Cycle Compensation (DCC)
- Advanced: Slew Time Control (STC)

Note

The advanced, adaptive drive functions and registers are not required for normal operation of the device and intended for specific system requirements.

Table 7-15. Smart Gate Driver Terminology Descriptions

Core Function	Terminology	Description
IDRIVE / TDRIVE	I_{DRVP}	Programmable gate drive source current for adjustable MOSFET slew rate control. Configured with the IDRVP_x control register or IDRIVE pin.
	I_{DRVN}	Programmable gate drive sink current for adjustable MOSFET slew rate control. Configured with the IDRVN_x control register or IDRIVE pin.
	I_{HOLD}	Fixed gate driver hold pull up current during non-switching period.
	I_{STRONG}	Fixed gate driver strong pull down current during non-switching period.
	t_{DRIVE}	$I_{DRVP/N}$ drive current duration before I_{HOLD} or I_{STRONG}. Also provides V_{GS} and V_{DS} fault monitor blanking period. Configured with the VGS_TDRV_x control register.
	t_{PD}	Propagation delay from logic control signal to gate driver output change.
	t_{DEAD}	Body diode conduction period between high-side and low-side switch transition. Configured with the VGS_TDEAD_x control register.

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Table 7-15. Smart Gate Driver Terminology Descriptions (continued)

Core Function	Terminology	Description
PDR (Pre-charge)	I_{CHR_INIT}	Gate drive source current initial value for charge control loop. Configured with the PRE_CHR_INIT_xx control register
	I_{PRE_CHR}	Gate drive source current for pre-charge period after control loop lock. Adjustment rate configured with the KP_PDR_x control register. Max current clamp configured with the PRE_MAX_x control register.
	t_{PRE_CHR}	Gate drive source current pre-charge period duration. Configured with the T_PRE_CHR_x control register.
	t_{DON}	Delay time from start of pre-charge period to rising V_{SH} crossing V_{SH_L} threshold. Configure with T_DON_DOFF_x control register.
	I_{DCHR_INIT}	Gate drive sink current initial value for discharge period control loop. Configured with the PRE_DCHR_INIT_x control register.
	I_{PRE_DCHR}	Gate drive sink current for pre-discharge period after control loop lock. Adjustment rate configured with the KP_PDR_x control register. Max current clamp configured with the PRE_MAX_x control register.
	t_{PRE_DCHR}	Gate drive sink current pre-discharge period duration. Configured with the T_PRE_DCHR_x control register.
	t_{DOFF}	Delay time from start of pre-discharge period to falling V_{SH} crossing V_{SH_H} threshold. Configure with T_DON_DOFF_x control register.
	V_{SH_L}	Low voltage threshold for V_{SH} switch-node. Configured with the AGD_THR control register.
	V_{SH_H}	High voltage threshold for V_{SH} switch-node. Configured with the AGD_THR control register.
PDR (Post-charge)	I_{PST_CHR}	Gate drive source current for post-charge period. Adjustment rate configured with the KP_PST_x control register.
	t_{PST_CHR}	Gate drive source current post-charge period duration.
	I_{PST_DCHR}	Gate drive sink current for post-discharge period. Adjustment rate configured with the KP_PST_x control register.
	t_{PST_DCHR}	Gate drive source current post-charge period duration.
	I_{FW_CHR}	Freewheeling charge current. Configured with the FW_MAX_x control register.
	I_{FW_DCHR}	Freewheeling discharge current. Configured with the FW_MAX_x control register.
STC	t_{RISE}	Time duration for V_{SHx} to cross from V_{SHx_L} to V_{SHx_H} threshold. Configured with the T_RISE_FALL_x control register.
	t_{FALL}	Time duration for V_{SHx} to cross from V_{SHx_H} to V_{SHx_L} threshold. Configured with the T_RISE_FALL_x control register.

7.3.4.1 Functional Block Diagram

Figure 7-11 shows a high level function block diagram for the half-bridge gate driver architecture. The gate driver blocks provide a variety of functions for MOSFET control, feedback, and protection. This includes complimentary, push-pull high-side and low-side gate drivers with adjustable drive currents, control logic level shifters, V_{DS}, V_{GS}, and V_{SH} (switch-node) feedback comparators, a high-side Zener clamp, plus passive and active pulldown resistors.

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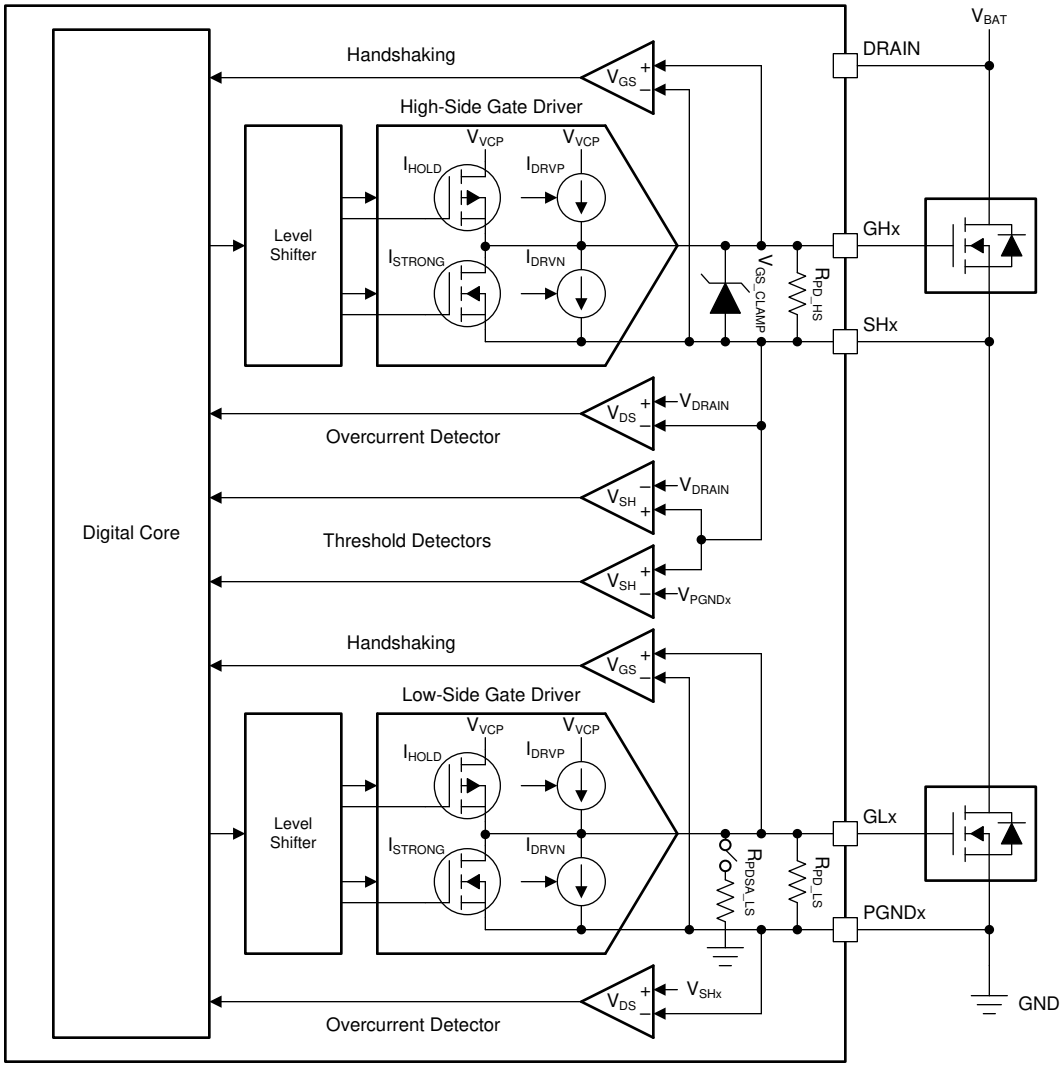

Figure 7-11. Gate Driver Functional Block Diagram

7.3.4.2 Slew Rate Control (IDRIVE)

The IDRIVE component of the smart gate drive architecture implements adjustable gate drive current control to adjust the external MOSFET V_{DS} slew rate. This is achieved by implementing adjustable pull up (I_{DRVP}) and pull down (I_{DRVN}) current sources for the internal gate driver architecture.

The external MOSFET V_{DS} slew rates are a critical factor for optimizing radiated and conducted emissions, diode reverse recovery, dV/dt parasitic gate coupling, and overvoltage or undervoltage transients on the switch-node of the half-bridge. IDRIVE operates on the principle that the V_{DS} slew rates are predominantly determined by the rate of the gate charge (or gate current) delivered during the MOSFET Q_{GD} or Miller charging region. By allowing the gate driver to adjust the gate current, it can effectively control the slew rate of the external power MOSFETs.

IDRIVE allows the DRV871x-Q1 to dynamically change the gate driver current setting through the IDRVP_x and IDRVN_x SPI registers or IDRIVE pin on H/W interface devices. The device provides 16 settings between the 0.5-mA and 62-mA range for the source and sink currents as shown in Table 7-16. The peak gate drive current is available for the t_{DRIVE} duration. After the MOSFET is switched and the t_{DRIVE} duration expires, the gate driver switches to a hold current (I_{HOLD}) for the pull up source current to limit the output current in case of a short circuit condition and to improve the efficiency of the driver.

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On SPI interface devices, the IDRV_LOx control register allows for 16 settings <0.5mA if extremely low slew rate control is required.

Table 7-16. IDRIVE Source (I_{DRVP}) and Sink (I_{DRVN}) Current

IDRVP_x / IDRVN_x	Gate Source / Sink Current	
	IDRV_LOx = 0b	IDRV_LOx = 1b
0000b	0.5 mA	50 µA
0001b	1 mA	110 µA
0010b	2 mA	170 µA
0011b	3 mA	230 µA
0100b	4 mA	290 µA
0101b	5 mA	350 µA
0110b	6 mA	410 µA
0111b	7 mA	600 µA
1000b	8 mA	725 µA
1001b	12 mA	850 µA
1010b	16 mA	1 mA
1011b	20 mA	1.2 mA
1100b	24 mA	1.4 mA
1101b	31 mA	1.6 mA
1110b	48 mA	1.8 mA
1111b	62 mA	2.3 mA

7.3.4.3 Gate Drive State Machine (TDRIVE)

The TDRIVE component of the smart gate drive architecture is an integrated gate drive state machine that provides automatic dead time insertion, parasitic dV/dt gate coupling prevention, and MOSFET gate fault detection.

The first component of the TDRIVE state machine is an automatic dead time handshake. Dead time is the period of body diode conduction time between the switching of the external high-side and low-side MOSFET to prevent any cross conduction or shoot through. The DRV871x-Q1 uses V_{GS} monitors to implement a break and then make dead time scheme by measuring the external MOSFET V_{GS} voltage to determine when to properly enable the external MOSFETs. This scheme allows the gate driver to adjust the dead time for variations in the system such as temperature drift, aging, voltage fluctuations, and variation in the external MOSFET parameters. An additional fixed digital dead time (t_{DEAD_D}) can be inserted if desired and is adjustable through the SPI registers.

The second component focuses on preventing parasitic dV/dt gate charge coupling. This is implemented by enabling a strong gate current pulldown (I_{STRONG}) whenever the opposite MOSFET in the half-bridge is switching. This feature helps remove parasitic charge that couples into the external MOSFET gate when the half-bridge switch node is rapidly slewing.

The third component implements a gate fault detection scheme to detect an issue with the gate voltage. This is used to detect pin-to-pin solder defects, a MOSFET gate failure, or a gate stuck high or stuck low voltage condition. This is done by using the V_{GS} monitors to measure the gate voltage after the end of the t_{DRIVE} time. If the gate voltage has not reached the proper threshold, the gate driver will report the corresponding fault condition. To ensure a false fault is not detected, a t_{DRIVE} time should be selected that is longer than the time required to charge or discharge the MOSFET gate. The t_{DRIVE} time does not impact the PWM minimum duration and will terminate early if another PWM command is received.

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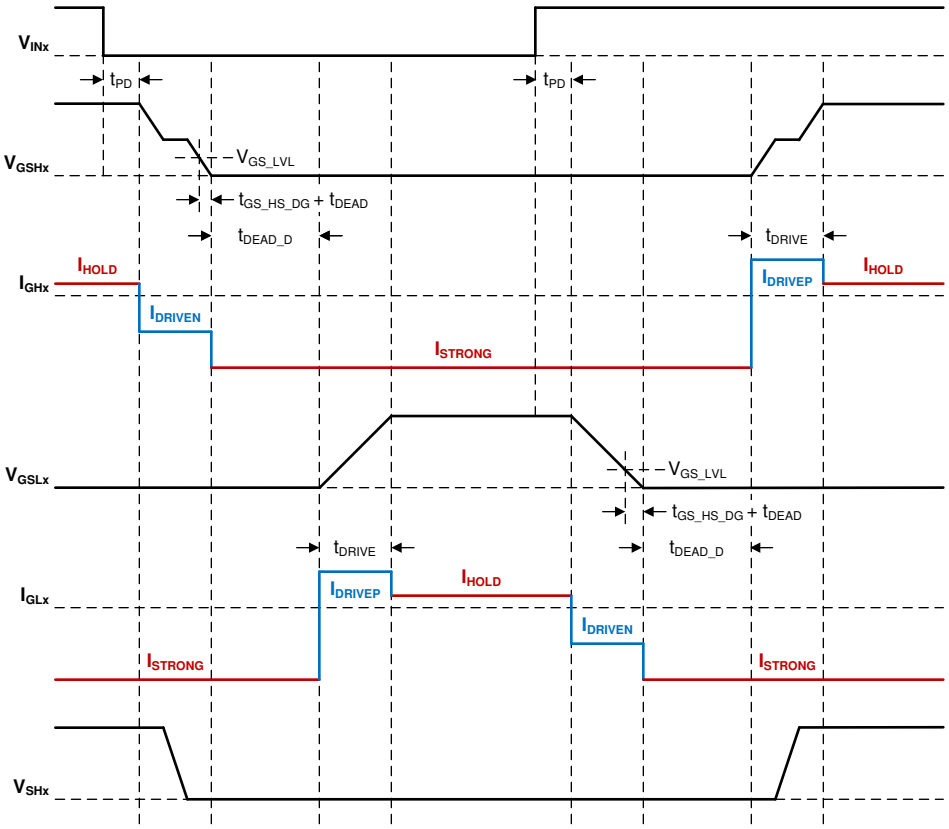

Figure 7-12. TDRIVE Turn On / Off

7.3.4.4 Propagation Delay Reduction (PDR)

Propagation delay reduction (PDR) control has two primary functions, a pre-charge propagation delay reduction function and a post-charge acceleration function. The PDR control function is only available in the Half-Bridge Control PWM mode and on SPI device variants.

The propagation delay reduction (PDR) primary goal is to reduce the turn on and turn off delay of the external MOSFET by using dynamic pre-charge and pre-discharge currents before the MOSFET Q_{GD} miller region. This can enable the driver to achieve higher and lower duty cycle resolution while still meeting difficult EMI requirements.

The post-charge acceleration function allows for the MOSFET to more quickly reach its low resistive or off state to minimize power losses by increasing the post-charge and post-discharge gate current after the MOSFET Q_{GD} miller region.

An example of the MOSFET pre-charge and post-charge current profiles are shown in Figure 7-13. The same control loop is repeated for the MOSFET pre-discharge and post-discharge as shown in Figure 7-14. Several examples of the full control loop in different PWM and motor cases are shown in Figure 7-15 and Figure 7-16.

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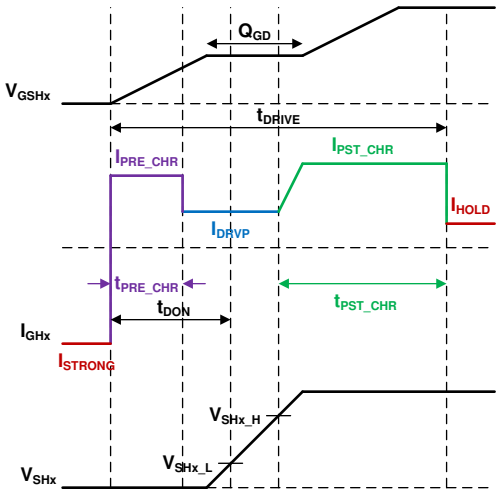

Figure 7-13. PDR Charge Profile

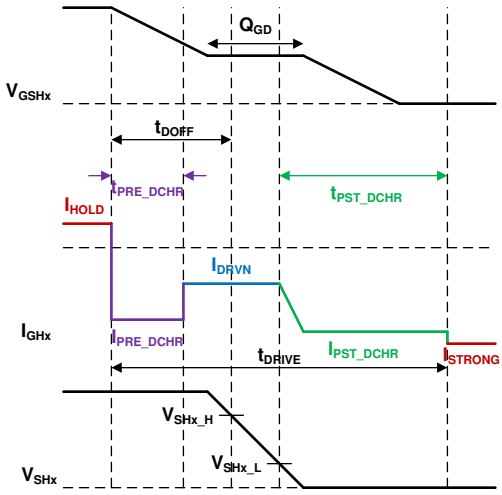

Figure 7-14. PDR Discharge Profile

7.3.4.4.1 PDR Pre-Charge/Pre-Discharge Control Loop Operation Details

The PDR pre-charge/pre-discharge control loop operates to achieve a user configured turn on and turn off propagation delay (T_DON_DOFF_x) by dynamically adjusting the driver pre-charge (I_{PRE_CHR}) and pre-discharge (I_{PRE_DCHR}) current levels through a proportional gain error controller (KP_PDR_x). The error controller measures the difference in the measured propagation delays (t_{ON}, t_{OFF}) compared to the configured propagation delay (T_DON_DOFF_x) and updates the pre-charge current level for the next switching cycle. The control loop can be operated with the default configuration settings of the device, but full flexibility is provided to configure the timing parameters, initial current levels, error controller strength, and other settings.

7.3.4.4.1.1 PDR Pre-Charge/Pre-Discharge Setup

- Enable the PDR control loop. EN_PDR_x register setting.
- Set the active PWM half-bridge (DRV8718-Q1 only). SET_AGD_x register setting. Note: The advance driver control settings are shared between each half-bridge pair (1/2, 3/4, 5/6, and 7/8) for DRV8718-Q1.
- Set the target t_{ON} and t_{OFF} propagation delay. T_DON_DOFF_x register setting. It is recommended to maintain a value greater than 700 ns to accommodate driver and system delays.
- **Optional Configuration Options:**
  - Adjust initial current values. PRE_CHR_INIT_x, PRE_DCHR_INIT_x register settings.
  - Adjust pre-charge and pre-discharge time duration. T_PRE_CHR_x, T_PRE_DCHR_x register settings.
  - Adjust the proportional gain controller strength. KP_PDR_x register setting.
  - Adjust the maximum current level threshold. PRE_MAX_x, register settings.

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7.3.4.4.2 PDR Post-Charge/Post-Discharge Control Loop Operation Details

The PDR post charge/post-discharge control loop operates by increasing the driver gate current after the MOSFET switching region. This is done by measuring the switch-node voltage (V_{SHx}) and then increasing gate current after crossing the proper threshold. The control loop can be operated with the default configuration settings of the device, but full flexibility is provided to configure the timing parameters, controller strength, and other settings.

7.3.4.4.2.1 PDR Post-Charge/Post-Discharge Setup

- Enable the post-charge/post-discharge control loop. KP_PST_x register setting.
- Set the active PWM half-bridge (DRV8718-Q1 only). SET_AGD_x register setting. Note: The advance driver control settings are shared between each half-bridge pair (1/2, 3/4, 5/6, and 7/8) for DRV8718-Q1.
- **Optional Configuration Options:**
  - Add additional delay before post-charge/post-discharge starts. EN_PST_DLY_xx register setting.
  - Adjust the proportional gain controller strength. KP_PST_x register setting.

7.3.4.4.3 Detecting Drive and Freewheel MOSFET

By default, the PDR loop automatically detects which MOSFET is the drive MOSFET and which MOSFET is the freewheel MOSFET by determining the polarity of the current out of the half-bridge. This is done by measuring the half-bridge V_{SHx} voltage during the dead-time period to determine if the high-side or low-side body diode is conducting. If the current polarity cannot be determined it is assumed that the configured MOSFET through PWMx_HL is the drive MOSFET. The automatic freewheel detection can be disabled with the IDIR_MAN_x control register. In the manual freewheel modes, the PDR loop relies on the PWMx_HL control register to determine which MOSFET is the drive MOSFET and which MOSFET is the freewheel MOSFET. IF PWMx_HL = 0b, the high-side MOSFET is the drive MOSFET and the low-side MOSFET is the freewheel MOSFET. If PWMx_HL = 1b, the low-side MOSFET is the drive MOSFET and high-side MOSFET is the freewheel MOSFET.

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Figure 7-15 shows the high-side MOSFET (HS1) controlling the V_{SHx} switch-node voltage transition and the low-side MOSFET (LS1) acting as the freewheeling MOSFET.

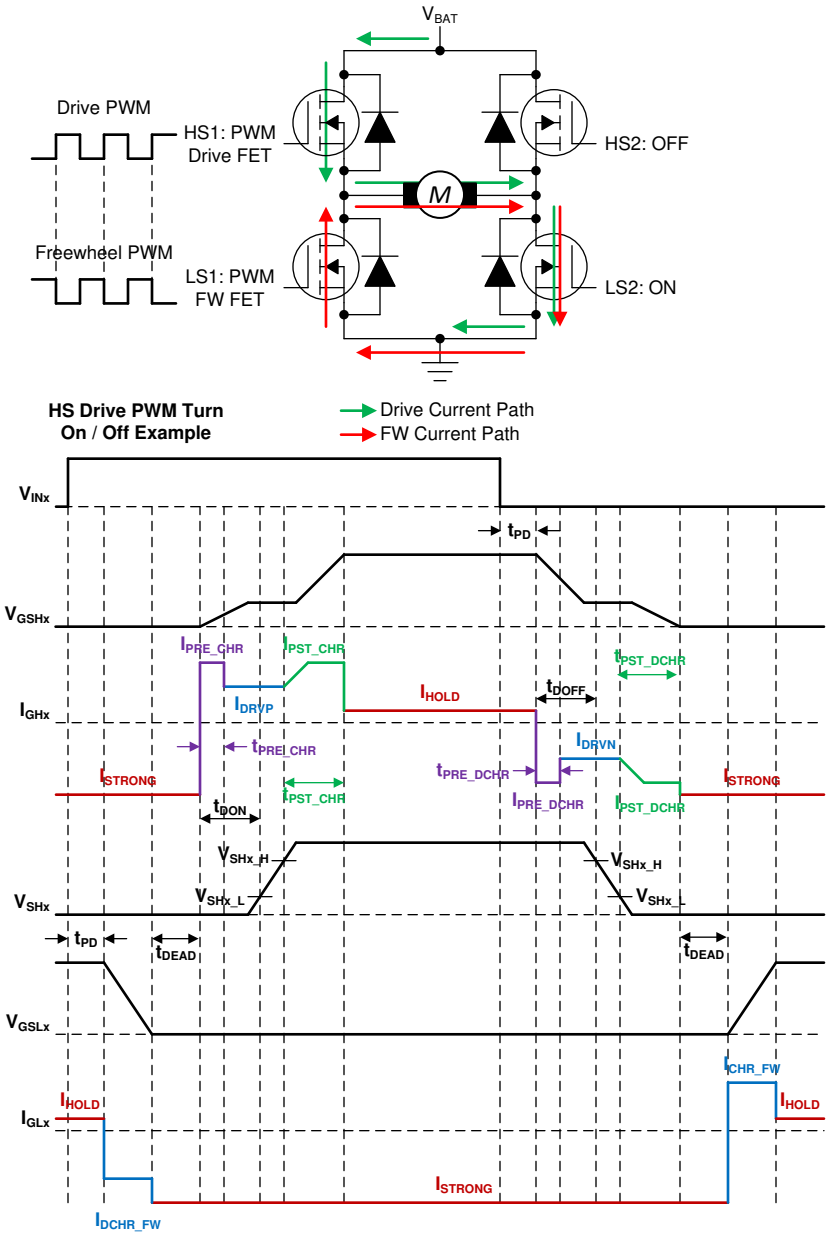

Figure 7-15. HS Drive PWM Turn On / Off Example

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Figure 7-16 shows the low-side MOSFET (LS2) controlling the V_{SHx} switch-node voltage transition and the high-side MOSFET (HS2) acting as the freewheeling MOSFET.

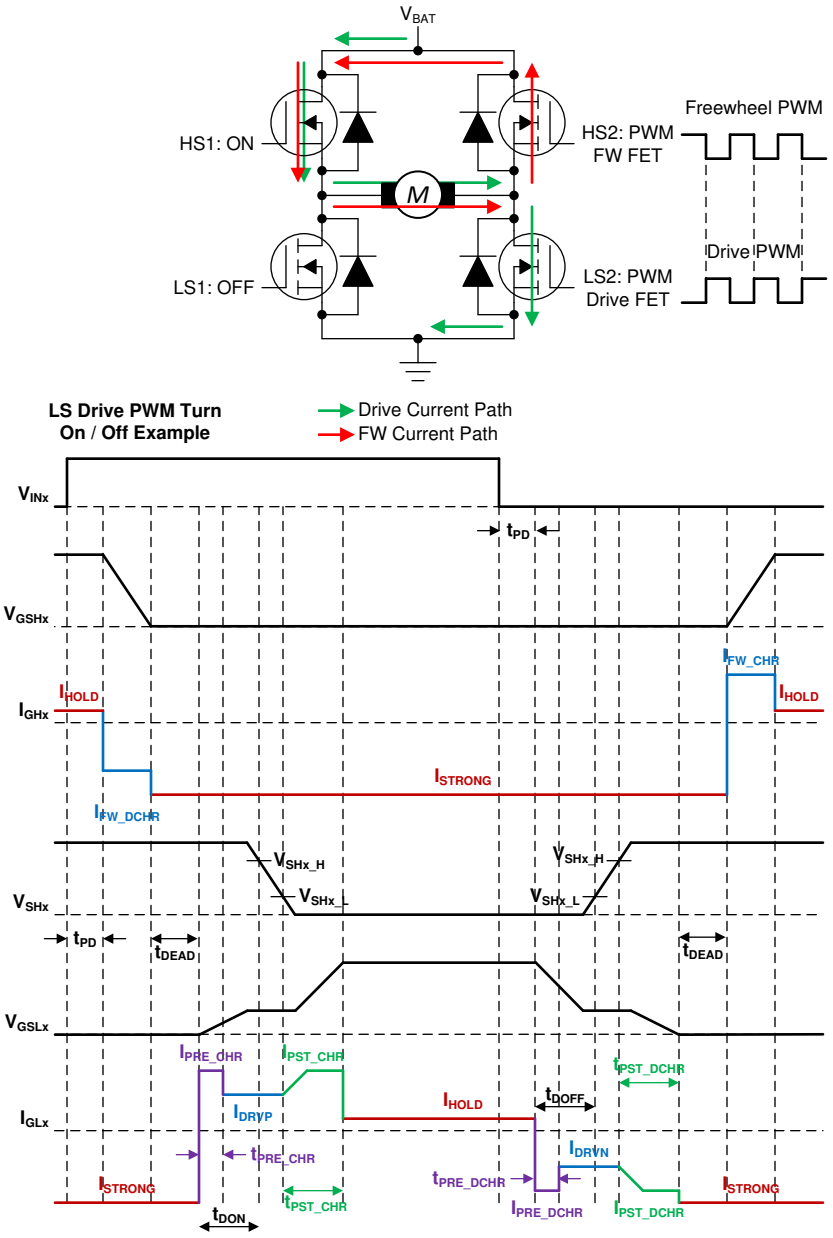

Figure 7-16. LS Drive PWM Turn On / Off Example

7.3.4.5 Automatic Duty Cycle Compensation (DCC)

The automatic duty cycle compensation (DCC) smart gate driver feature is a function to match the turn on and turn off signals in order to reduce duty cycle distortion that occurs due to different delays in the turn on and turn off sequences. The difference in turn on and turn off delay is introduced by a dependancy on whether the freewheeling MOSFET must be charged or discharged before the V_{SHx} slew can occur. If the freewheeling MOSFET charges or discharges before the drive MOSFET this can introduce a mismatch causing duty cycle distortion. The DCC control loop adds an additional delay to match both the turn on and turn off delays. This function can be utilized in the standard drive modes or in combination with the PDR or STC control modes.

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The DCC function is enabled through the EN_DCC_xx register setting. Set the active half-bridge that will receive PWM control through the SET_AGD_xx register setting (DRV8718-Q1 only).

7.3.4.6 Closed Loop Slew Time Control (STC)

The slew time control (STC) loop provides the device the ability to configure a specific slew rise and fall time for the output switch-node. The device will adjust the gate drive output current (I_{DRVP} and I_{DRVN}) to meet the desired target settings. This function can be utilized in the standard drive modes or in combination with the PDR or DCC control modes.

7.3.4.6.1 STC Control Loop Setup

- Enable the STC control loop. EN_STC_x register setting
- Set the active PWM half-bridge (DRV8718-Q1 only). SET_AGD_x register setting. Note: The advance driver control settings are shared between each half-bridge pair (1/2, 3/4, 5/6, and 7/8) for DRV8718-Q1.
- Set the target t_{RISE} and t_{FALL} time. T_RISE_FALL_x register setting.
- **Optional Configuration Options:**
- Adjust the proportional gain controller strength. KP_STC_x register setting.

7.3.5 Tripler (Dual-Stage) Charge Pump

The high-side gate drive voltage for the external MOSFET is generated using a tripler (dual-stage) charge pump that operates from the PVDD voltage supply input. The charge pump allows the high-side and low-side gate drivers to properly bias the external N-channel MOSFETs with respect to its source voltage across a wide input supply voltage range. The charge pump output is regulated (V_{VCP}) to maintain a fixed voltage respect to V_{PVDD}. The charge pump is continuously monitored for an undervoltage (V_{CP_UV}) event to prevent under driven MOSFET conditions or in case of a short circuit condition.

The charge pump provides several configuration options. By default the charge pump will automatically switch between tripler (dual-stage) mode and doubler (single-stage) mode after the PVDD pin voltage crosses the V_{CP_SO} threshold in order to reduce power dissipation. On SPI device variants, the charge pump can also be configured to always remain in tripler or doubler mode through the SPI register setting CP_MODE.

The charge pumps requires a low ESR, 1-µF, 16-V ceramic capacitor (X5R or X7R recommended) between the PVDD and VCP pins to act as the storage capacitor. Additionally, a low ESR, 100-nF, PVDD-rated ceramic capacitor (X5R or X7R recommended) is required between the CP1H to CP1L and CP2H to CP2L pins to act as the flying capacitors.

Note

Since the charge pump is regulated to the PVDD pin, it should be ensured that the voltage difference between the PVDD pin and MOSFET power supply is limited to a threshold that allows for proper V_{GS} of the external MOSFET during switching operation.

7.3.6 Wide Common-Mode Current Shunt Amplifiers

The DRV871x-Q1 integrates two high-performance, wide common-mode, bidirectional, current-shunt amplifiers for current measurements using shunt resistors in the external half-bridges. Current measurements are commonly used to implement overcurrent protection, external torque control, or commutation with an external controller. Due to the high common-mode range of the shunt amplifier it can support low-side, high-side, or inline shunt configurations. The current shunt amplifiers include features such as programmable gain, unidirectional and bidirectional support, output blanking, and a dedicated voltage reference pin (AREF) to set a mid point bias voltage for the amplifier output. A simplified block diagram is shown in Figure 7-17. SPx should connect to the positive terminal of the shunt resistor and SNx should connect to the negative terminal of the shunt resistor. If the amplifiers are not utilized, the AREF, SNx, SPx inputs can be tied to AGND, AGND to PCB GND and the SOx outputs left floating.

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Note

It should be noted that in high-side sense configuration there exists a leakage path of approximately 600kΩ to GND when nSLEEP = 0V.

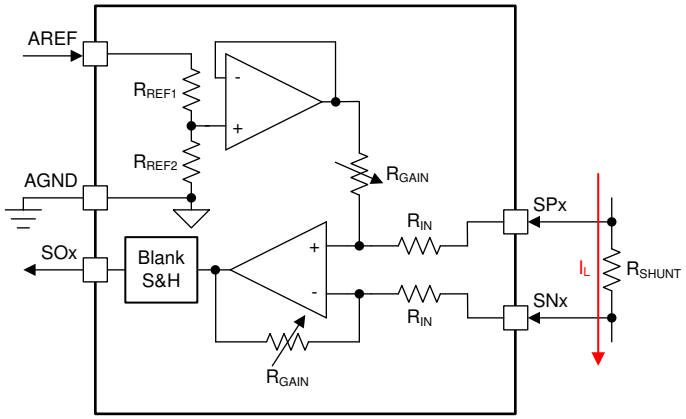

Figure 7-17. Amplifier Simplified Block Diagram

A detailed block diagram is shown in Figure 7-18. The wide common mode amplifier is implemented with a two stage differential architecture. The 1st differential stage supports a wide common mode input, differential output, and has a fixed gain, G = 2. The 2nd differential stage supports a variable gain adjustment, G = 5, 10, 20, or 40. The total gain of the two stages will be G = 10, 20, 40, or 80.

The amplifier can also generate an output voltage bias through the AREF pin. The AREF pin goes to a divider network, a buffer, and then sets the output voltage bias for the differential amplifier. On SPI device variants, the gain is configured through the register setting CSA_GAIN and the reference division ratio through CSA_DIV. On H/W device variants, the reference division ratio is fixed to V_{AREF} / 2. The gain is configured through the GAIN pin.

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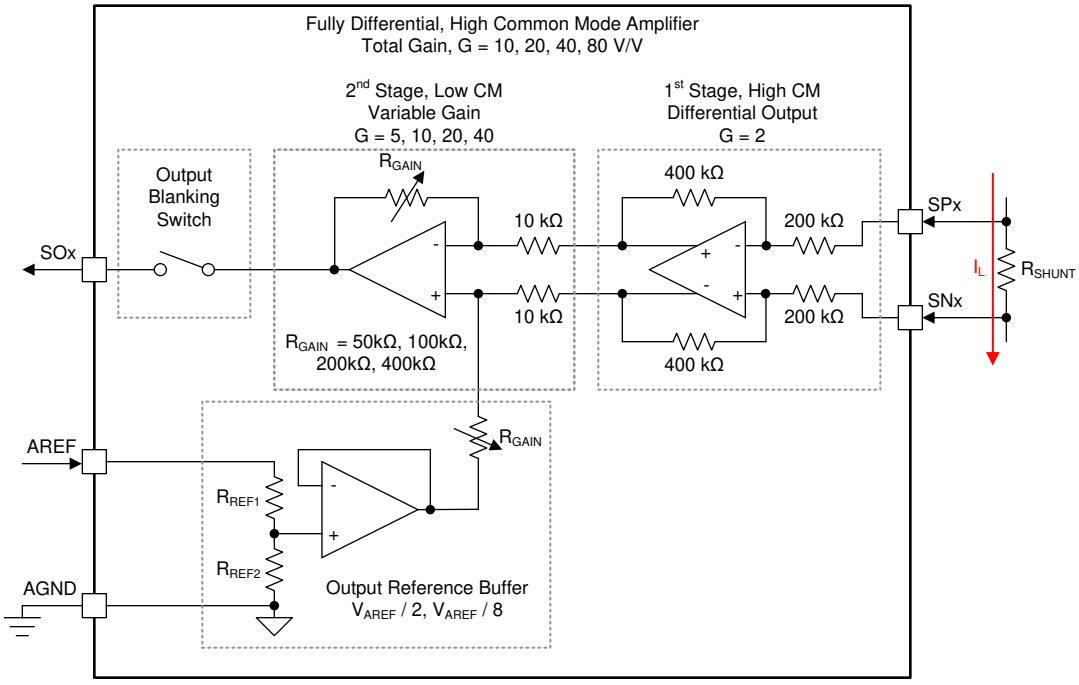

Figure 7-18. Amplifier Detailed Block Diagram

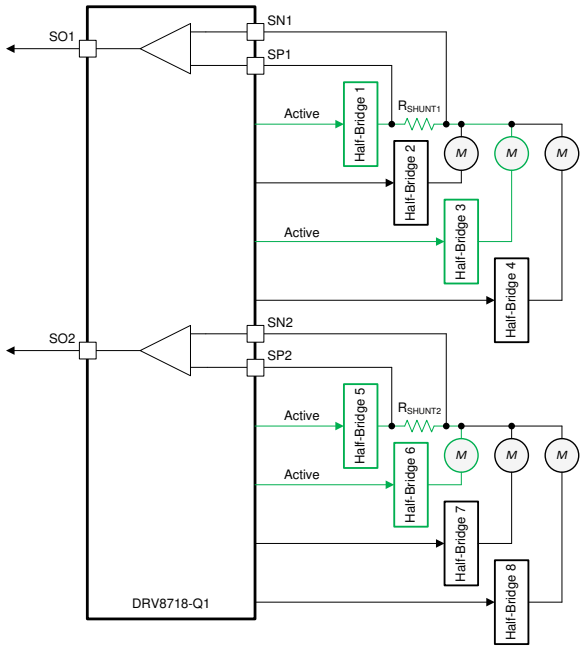

Figure 7-19. Shared Shunt Resistor

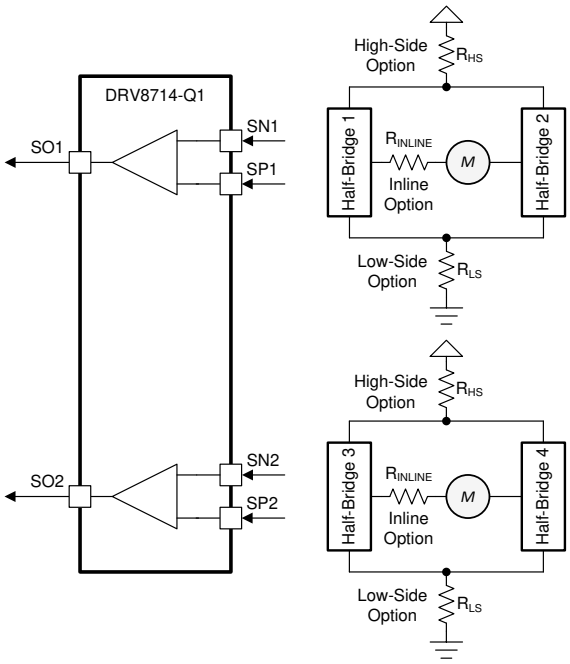

Figure 7-20. Individual H-Bridge Shunt Resistor

The DRV8718-Q1 inline shunt amplifier can be used to continuously sense motor current even in shared group or zone control configurations. The DRV8714-Q1 provides two shunt amplifiers for the four half-bridge gate drivers allowing for individual H-bridge current sensing if the system requires.

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Lastly, the amplifier has an output blanking switch. This option is only available on SPI device variants. The output switch can be used to disconnect the amplifier output during PWM switching to reduce output noise (blanking). The blanking circuit can be set trigger on the active half-bridge (half-bridge 1-8) through the CSA_BLK_SEL_x register setting. The blanking period can be configured through the CSA_BLK_x register setting. If the gate drivers are transitioning between high-side and low-side FET turn on and turn off or vice versa, the blanking time will extend through the dead-time window to avoid amplifier signal noise if the output swings or noise couples during the dead-time period. An output hold up capacitor is recommended to stabilize the amplifier output when it is disconnected during blanking. Typically this capacitor should be after a series resistor in a RC filter configuration to limit direct capacitance seen directly at the amplifier output. An example of the blanking function is shown in Figure 7-21.

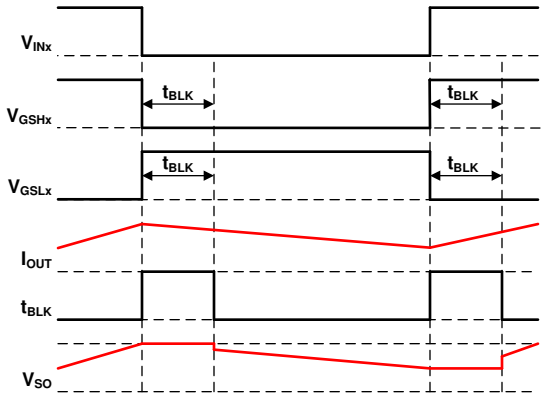

Figure 7-21. Amplifier Blanking Example

7.3.7 Pin Diagrams

This section presents the I/O structure of all the digital input and output pins.

7.3.7.1 Logic Level Input Pin (INx/ENx, INx/PHx, nSLEEP, nSCS, SCLK, SDI)

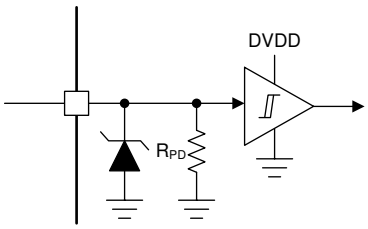

Figure 7-22. Input Pin Structure

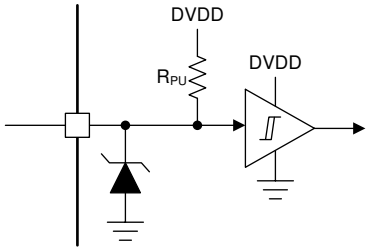

Figure 7-23. Input Pin Structure (nSCS)

7.3.7.2 Logic Level Push Pull Output (SDO)

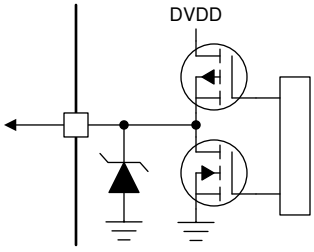

Figure 7-24. Push Pull Output Structure (SDO)

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7.3.7.3 Logic Level Multi-Function Pin (DRVOFF/nFLT)

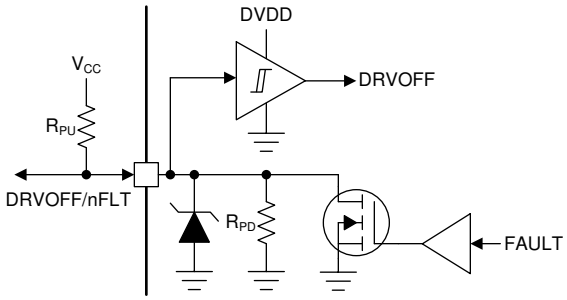

Figure 7-25. Multi-Function Pin Structure (DRVOFF/nFLT)

7.3.7.4 Quad-Level Input (GAIN, MODE)

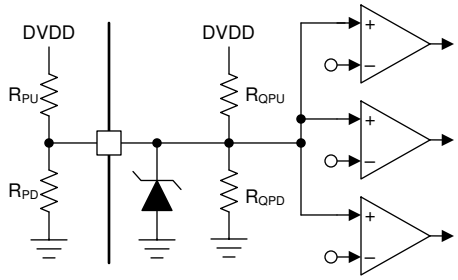

Figure 7-26. Quad-Level Input Structure (GAIN, MODE)

7.3.7.5 Six-Level Input (IDRIVE, VDS)

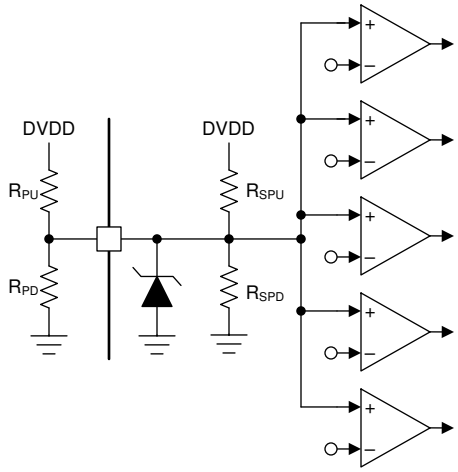

Figure 7-27. Six-Level Input Structure (IDRIVE, VDS)

7.3.8 Protection and Diagnostics

7.3.8.1 Gate Driver Disable (DRVOFF/nFLT and EN_DRV)

The DRV871x-Q1 provides dedicated driver disable functions with the DRVOFF/nFLT pin and EN_DRV SPI register bit on SPI device variants. When DRVOFF/nFLT or EN_DRV are asserted, all half-bridges will be set Hi-Z by enabling the gate driver pull downs regardless of the other pin or SPI inputs.

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The EN_DRV SPI register bit is provided for a controlled power up sequence. After device power up all the half-bridges remain disabled (all pulldowns active, EN_DRV = 0b) until the EN_DRV register bit is asserted high. This allows for the system to power up and conduct configuration sequences before the gate drivers are enabled. On H/W devices, this functionality is not provided and the driver will automatically enable after power up.

The DRVOFF/nFLT pin provides a direct hardware pin to shutdown the output drivers without relying on an SPI command or PWM input change.

The DRVOFF/nFLT pin is a multi-function configurable pin. By default, the pin functions as a global driver disable. If this function is not required, the pin be changed to an open-drain fault interrupt for the MCU through the device DRVOFF_nFLT register setting. When configured as DRVOFF, a logic high input will disable the drivers and logic low will allow for normal operation.

7.3.8.2 Low I_Q Powered Off Braking (POB, BRAKE)

The DRV871x-Q1 provide the ability to enable the low-side gate drivers while the device is in its low-power sleep mode (nSLEEP = logic low). This allows the external low-side power MOSFETs to be enabled while maintaining a low quiescent current draw from the power supply. Enabling the external low-side MOSFETs allows the device to actively brake a motor connected to the external half-bridges by shorting the back emf across the motor terminals. This can help prevent reverse driving of the motor by an external force from overcharging the system power supply by dissipating the energy in the low-side MOSFETs. This function is only available while the device is in its low-power sleep mode. The function is enabled by taking the BRAKE pin to logic high.

The powered off braking function is available on half-bridges 5, 6, 7, and 8 on the DRV8718-Q1 device. On the DRV8714-Q1, the power off braking function is available on all four half-bridges. The BRAKE pin will enable or disable the low-side gate drivers for all four of the half-bridges together. The powered off braking function requires the PVDD voltage supply to be present in order to enable the low-side gate drivers, but the function can operate without the DVDD logic power supply present.

In case of a short circuit to power supply fault present on the power stage, a simple overcurrent detector circuit with analog RC deglitch filter is provided to disable the low-side MOSFET if a high current event is detected while braking. This is needed since the normal overcurrent protection circuits are disabled during the device low-power sleep mode. The overcurrent comparator and RC deglitch filter values are fixed and cannot be adjusted.

The powered off braking function is enabled through the BRAKE pin and the BRAKE pin can be pulled high through several different methods. To reduce quiescent current draw, the pulldown resistance of the BRAKE pin is reduced to 1MOhm while in device low-power sleep mode. The BRAKE pin can be always left high while the device is in low-power sleep mode or can be set high in response to a rising voltage on the power supply. The BRAKE pin has an internal voltage clamp allowing it to be connected directly to the PVDD battery supply through a Zener diode (to set overvoltage threshold) with a series resistor to limit the current. The powered off function can be set to automatically enable in low-power sleep mode by leaving the BRAKE pin disconnected and relying on the internal overvoltage monitor.

Some methods to pull up the BRAKE pin and enable the powered off braking function include:

- Option 1: Internal overvoltage monitor. BRAKE pin should be left not-connected (Hi-Z)
- Option 2: Voltage triggered pull up with passive Zener diode. An external Zener diode can be added to the BRAKE pin to create an overvoltage trigger that is lower than the internal overvoltage monitor.
- Option 3: MCU fixed digital output high or MCU digital output in response to motor movement detected by senor or rising voltage. A digital output to the BRAKE pin can directly control whether the power off braking function is enabled (LO = disabled, HI = enabled).
- Option 4: The power off braking function can be disabled by shorting/connecting the BRAKE pin directly to PCB ground.

By default (BRAKE pin not connected), the powered off braking function is enabled by an internal overvoltage monitor that will detect the PVDD voltage and enable the low-side braking if voltage crosses the comparator

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threshold. The internal overvoltage monitor and power off braking function can be disabled by shorting the BRAKE pin directly to PCB ground.

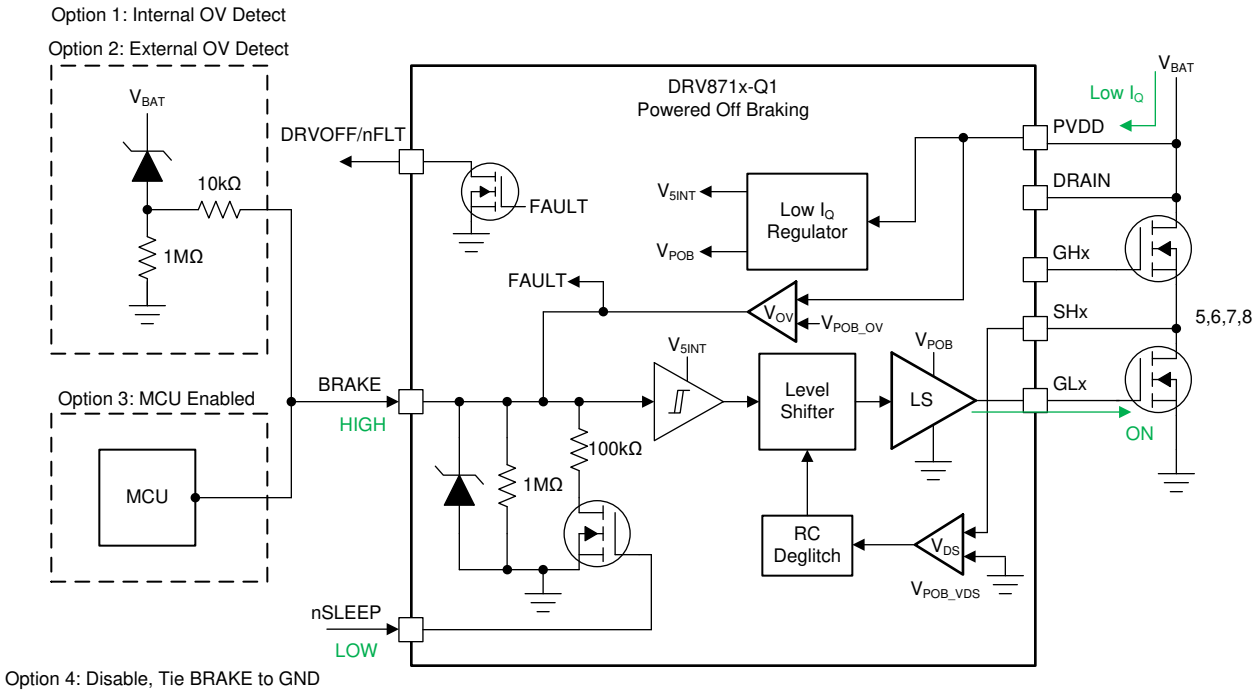

Figure 7-28. Powered Off Braking

Note

If the powered off braking function is not utilized, the BRAKE pin should be connected directly to GND.

7.3.8.3 Fault Reset (CLR_FLT)

The DRV871x-Q1 provides a specific sequence to clear fault conditions from the driver and resume operation. This function is provided through the CLR_FLT register bit. To clear fault reporting the CLR_FLT register bit must be asserted after the fault condition is removed. After being asserted, the driver will clear the fault and reset the CLR_FLT register bit. The function is only available on SPI device variants. On H/W device variants, all faults will automatically recover once the condition is removed.

7.3.8.4 DVDD Logic Supply Power on Reset (DVDD_POR)

If at any time the input logic supply voltage on the DVDD pin falls below the V_{DVDD_POR} threshold for longer than the $t_{DVDD_POR_DG}$ time or the nSLEEP pin is asserted low, the device enter its inactive state disabling the gate drivers, charge pump, and protection monitors. Normal operation resumes when the DVDD undervoltage condition is removed or the nSLEEP pin is asserted high. After a DVDD power on reset (POR), the POR register bit is asserted until CLR_FLT is issued.

7.3.8.5 PVDD Supply Undervoltage Monitor (PVDD_UV)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD_UV_DG}$ time, the DRV871x-Q1 detects a PVDD undervoltage condition. After detecting the undervoltage condition, the gate driver pull downs are enabled, charge pump disabled and nFAULT pin, FAULT register bit, and PVDD_UV register bit asserted.

On SPI device variants, the PVDD undervoltage monitor can recover in two different modes set through the PVDD_UV_MODE register setting.

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- **Latched Fault Mode:** After the undervoltage condition is removed, the fault state remains latched and charge pump disabled until CLR_FLT is issued.
- **Automatic Recovery Mode:** After the undervoltage condition is removed, the nFAULT pin and FAULT register bit are automatically cleared and the charge pump automatically reenabled. The PVDD_UV register bit remains latched until CLR_FLT is issued.

On H/W device variants, the PVDD undervoltage monitor is fixed to automatic recovery mode.

7.3.8.6 PVDD Supply Overvoltage Monitor (PVDD_OV)

If the power supply voltage on the PVDD pin exceeds the V_{PVDD_OV} threshold for longer than the $t_{PVDD_OV_DG}$ time, the DRV871x-Q1 detects a PVDD overvoltage condition and action is taken according to the PVDD_OV_MODE register setting. The overvoltage threshold and deglitch time can be adjusted through the PVDD_OV_LVL and PVDD_OV_DG register settings.

On SPI device variants, the PVDD overvoltage monitor can respond and recover in four different modes set through the PVDD_OV_MODE register setting.

- **Latched Fault Mode:** After detecting the overvoltage condition, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and PVDD_OV register bit asserted. After the overvoltage condition is removed, the fault state remains latched until CLR_FLT is issued.
- **Automatic Recovery Mode:** After detecting the overvoltage condition, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and PVDD_OV register bit asserted. After the overvoltage condition is removed, the nFAULT pin and FAULT register bit are automatically cleared and the driver automatically reenabled. The PVDD_OV register bit remains latched until CLR_FLT is issued.
- **Warning Report Only Mode:** The PVDD overvoltage condition is reported in the WARN and PVDD_OV register bits. The device will not take any action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The PVDD overvoltage monitor is disabled and will not respond or report.

On H/W device variants, the PVDD overvoltage monitor is disabled.

7.3.8.7 VCP Charge Pump Undervoltage Lockout (VCP_UV)

If at any time the voltage on the VCP pin falls below the V_{VCP_UV} threshold for longer than the $t_{VCP_UV_DG}$ time, the DRV871x-Q1 detects a VCP undervoltage condition. After detecting the undervoltage condition, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and VCP_UV register bit asserted. The undervoltage threshold can be adjusted through the VCP_UV_LVL register setting.

On SPI device variants, the VCP undervoltage monitor can recover in two different modes set through the VCP_UV_MODE register setting.

- **Latched Fault Mode:** Additionally the charge pump is disabled in latched fault mode. After the undervoltage condition is removed, the fault state remains latched and charge pump disabled until CLR_FLT is issued.
- **Automatic Recovery Mode:** After the undervoltage condition is removed, the nFAULT pin and FAULT register bit are automatically cleared and the driver automatically reenabled. The VCP_UV register bit remains latched until CLR_FLT is issued.

On H/W device variants, the VCP undervoltage monitor is fixed to automatic recovery mode and the threshold to 2-V.

7.3.8.8 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

If the voltage across the V_{DS} overcurrent comparator exceeds the V_{DS_LVL} for longer than the t_{DS_DG} time, the DRV871x-Q1 detects a V_{DS} overcurrent condition. The voltage threshold and deglitch time can be adjusted through the VDS_LVL and VDS_DG register settings. Additionally, in independent half-bridge and DRV8714-Q1 split HS/LS PWM control (BRG_MODE = 00b, 11b) the device can be configured to disable all half-bridges or only the associated half-bridge in which the fault occurred through the VDS_IND register setting. In the DRV8714-Q1 PH/EN and PWM H-bridge control modes (BRG_MODE = 01b, 10b), the VDS_IND register setting can be used to disable all H-bridges or only the associated H-bridge in which the fault occurred.

On SPI device variants, the V_{DS} overcurrent monitor can respond and recover in four different modes set through the VDS_MODE register setting.

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- **Latched Fault Mode:** After detecting the overcurrent event, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and associated VDS register bit asserted. After the overcurrent event is removed, the fault state remains latched until CLR_FLT is issued.
- **Cycle by Cycle Mode:** After detecting the overcurrent event, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and associated VDS register bit asserted. The next PWM input will clear the nFAULT pin and FAULT register bit and reenable the driver automatically. The associated VDS register bit will remain asserted until CLR_FLT is issued.
- **Warning Report Only Mode:** The overcurrent event is reported in the WARN and associated VDS register bits. The device will not take any action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The V_{DS} overcurrent monitors are disabled and will not respond or report.

On H/W device variants, the V_{DS} overcurrent mode is fixed to cycle by cycle and t_{VDS_DG} is fixed to 4 µs. Independent half-bridge shutdown is automatically enabled for the independent half-bridge and split HS/LS PWM control modes. Independent H-bridge shutdown is automatically enabled for the H-bridge PWM control modes. Additionally, the V_{DS} overcurrent protection can be disabled through level 6 of the VDS pin multi-level input.

When a V_{DS} overcurrent fault occurs, the gate pull down current can be configured in order to increase or decrease the time to disable the external MOSFET. This can help to avoid a slow-turn off during high-current short circuit conditions. This setting is configure through the VDS_IDRVN register setting on SPI devices. On hardware devices, this setting is automatically matched to the programmed I_{DRVN} current.

7.3.8.9 Gate Driver Fault (VGS_GDF)

If the V_{GS} voltage does not cross the the V_{GS_LVL} comparator level for longer than the t_{DRIVE} time, the DRV871x-Q1 detects a V_{GS} gate fault condition. Additionally, in independent half-bridge and DRV8714-Q1 split HS/LS PWM control (BRG_MODE = 00b, 11b) the device can be configured to disable all half-bridges or only the associated half-bridge in which the gate fault occurred through the VGS_IND register setting. In the DRV8714-Q1 PH/EN and PWM H-bridge control modes (BRG_MODE = 01b, 10b), the VGS_IND register setting can be used to disable all H-bridges or only the associated H-bridge in which the fault occurred.

On SPI device variants, the V_{GS} gate fault monitor can respond and recover in four different modes set through the VGS_MODE register setting.

- **Latched Fault Mode:** After detecting the gate fault event, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and associated VGS register bit asserted. After the gate fault event is removed, the fault state remains latched until CLR_FLT is issued.
- **Cycle by Cycle Mode:** After detecting the gate fault event, the gate driver pull downs are enabled and nFAULT pin, FAULT register bit, and associated VGS register bit asserted. The next PWM input will clear the nFAULT pin and FAULT register bit and reenable the driver automatically. The associated VGS register bit will remain asserted until CLR_FLT is issued.
- **Warning Report Only Mode:** The overcurrent event is reported in the WARN and associated VGS register bits. The device will not take any action. The warning remains latched until CLR_FLT is issued.
- **Disabled Mode:** The V_{GS} gate fault monitors are disabled and will not respond or report.

On H/W device variants, the V_{GS} gate fault mode is fixed to cycle by cycle and t_{DRIVE} is fixed to 4 µs. Independent half-bridge shutdown is automatically enabled for the independent half-bridge and split HS/LS PWM control modes. Independent H-bridge shutdown is automatically enabled for the H-bridge PWM control modes. Additionally, the V_{GS} gate fault protection can be disabled through level 6 of the VDS pin multi-level input.

7.3.8.10 Thermal Warning (OTW)

If the die temperature exceeds the T_{OTW} thermal warning threshold the DRV871x-Q1 detects an overtemperature warning and asserts the WARN and OTW register bits. After the overtemperature condition is removed the WARN and OTW register bits remain asserted until CLR_FLT is issued.

On H/W device variants, the overtemperature warning is not detected or reported.

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7.3.8.11 Thermal Shutdown (OTSD)

If the die temperature exceeds the T_{OTSD} thermal shutdown threshold the DRV871x-Q1 detects an overtemperature fault. After detecting the overtemperature fault, the gate driver pull downs are enabled, the charge pump disabled and nFAULT pin, FAULT register bit, and OTSD register bit asserted. After the overtemperature condition is removed the fault state remains latched until CLR_FLT is issued.

On H/W device variants, after the overtemperature condition is removed, the nFAULT pin is automatically cleared and the driver and charge pump automatically reenabled.

7.3.8.12 Offline Short Circuit and Open Load Detection (OOL and OSC)

The device provides the necessary hardware to conduct offline short circuit and open load diagnostics of the external power MOSFETs and load. This is accomplished by an integrated pull up and pull down current source on the SHx pin which connect to the external half-bridge switch-node. The offline diagnostics are controlled by the associated registers bits in the OLSC_CTRL register. First, the offline diagnostic mode needs to be enabled through the EN_OLSC register setting. Then the individual current sources can be enabled through the PD_SHx and PU_SHx register settings.

The voltage on the SHx pin will be continuously monitored through the internal V_{DS} comparators. During the diagnostic state the V_{DS} comparators will report the real-time voltage feedback on the SHx pin node in the SPI registers in the associated VDS register status bit. When in the V_{DS} comparators are in diagnostic mode, the global DS_GS SPI register bits will not report faults or warnings.

Before enabling the offline diagnostics it is recommended to place the external MOSFET half-bridges in the disabled state through the EN_DRV register setting. Additionally, the V_{DS} comparator threshold (VDS_LVL) should be adjusted to 1-V or greater to ensure enough headroom for the internal blocking diode forward voltage drop.

On H/W device variants, this feature is not available.

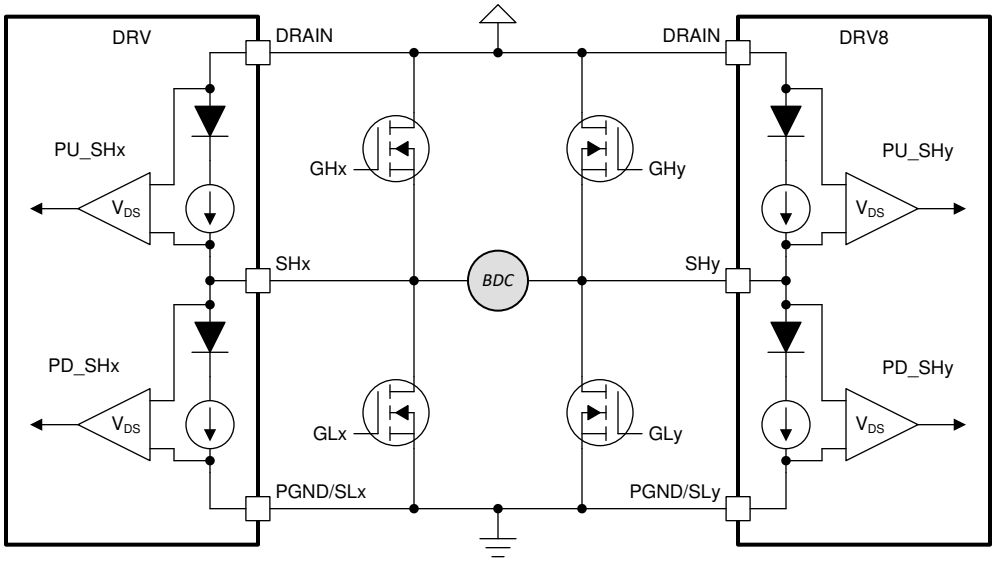

Figure 7-29. Offline Diagnostics

Note

The V_{DS} comparators will start real-time voltage feedback immediately after OLSC_EN is set. Feedback should be ignored until the proper pull up and pull down configuration is set.

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7.3.8.13 Watchdog Timer

The device integrates a programmable window type SPI watchdog timer to verify that the external controller is operating and the SPI bus integrity is monitored. The SPI watchdog timer can be enabled by through the WD_EN SPI register bit. The watchdog timer is disabled by default. When the watchdog timer is enabled, an internal timer starts to count up. The watcher dog timer is reset by inverting the WD_RST SPI register.. This WD_RST must be issued between the lower window time and the upper window time. If a watchdog timer fault is detected, the device response can be configured to either report only a warning or report a fault and disabled the half-bridge drivers. If the watchdog is set to disable the half-bridges drivers, the drivers will be reenabled after a CLR_FLT command is sent to remove the watchdog fault condition.

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7.3.8.14 Fault Detection and Response Summary Table

Table 7-17. Fault Detection and Response Summary

NAME	CONDITION	SPI BIT	MODE	DIGITAL CORE	CHARGE PUMP	GATE DRIVERS	CURRENT SENSE	RESPONSE
Disable Driver	DRVOFF = High or EN_DRV = 0b	n/a	n/a	Active	Active	Pull Down	Active	n/a
SPI Clock Fault	Invalid SPI Lock Frame	SCLK_FLT	Latched	Active	Active	Active	Active	SPI, Reject Frame
DVDD Power-on-Reset	DVDD < V_{DVDD_POR}	POR	n/a	Reset	Disabled	Semi-Active Pull Down	Disabled	SPI
PVDD Undervoltage	PVDD < V_{PVDD_UV}	UV, PVDD_UV	Latched	Active	Disabled	Semi-Active Pull Down	Disabled	nFAULT, SPI
			Automatic	Active	Disabled	Semi-Active Pull Down	Disabled	nFAULT, SPI
PVDD Overvoltage	PVDD > V_{PVDD_UV}	OV, PVDD_OV	Latched	Active	Active	Pull Down	Active	nFAULT, SPI
		OV, PVDD_OV	Automatic	Active	Active	Pull Down	Active	nFAULT, SPI
		OV, PVDD_OV	Warning	Active	Active	Active	Active	WARN, SPI
		n/a	Disabled	Active	Active	Active	Active	n/a
VCP Undervoltage	VCP < V_{VCP_UV}	UV, VCP_UV	Latched	Active	Disabled	Semi-Active Pull Down	Disabled	nFAULT, SPI
			Automatic	Active	Active	Semi-Active Pull Down	Disabled	nFAULT, SPI
VDS Overcurrent	VDS > V_{VDS_LVL}	DS_GS, VDS_X	Latched	Active	Active	I_{VDS_IDRVN} Pull Down	Active	nFAULT, SPI
			Cycle	Active	Active	I_{VDS_IDRVN} Pull Down	Active	nFAULT, SPI
			Warning	Active	Active	Active	Active	WARN, SPI
			Disabled	Active	Active	Active	Active	n/a
VGS Gate Fault	VGS > V_{VGS_LVL}	DS_GS, VGS_X	Latched	Active	Active	Pull Down	Active	nFAULT, SPI
			Cycle	Active	Active	Pull Down	Active	nFAULT, SPI
			Warning	Active	Active	Active	Active	WARN, SPI
			Disabled	Active	Active	Active	Active	n/a
Thermal Warning	T_J > T_{OTW}	OT, OTW	Automatic	Active	Active	Active	Active	WARN, SPI
Thermal Shutdown	T_J > T_{OTSD}	OT, OTSD	Latched	Active	Disabled	Semi-Active Pull Down	Disabled	nFAULT, SPI
Offline Open Load	n/a	VDS_X	MCU	Active	Active	Pull Down	Active	SPI
Offline Short Circuit	n/a	VDS_X	MCU	Active	Active	Pull Down	Active	SPI
Watchdog	Invalid Access or Expiration	WD_FLT	Warning	Active	Active	Active	Active	WARN, SPI
			Latched Fault	Active	Active	Pull Down	Active	nFAULT, SPI

7.4 Device Functional Modes

7.4.1 Inactive or Sleep State

When the nSLEEP pin is logic low or the DVDD power supply is below the V_{DVDD_POR} threshold, the device enters a low power sleep state to reduce device quiescent current draw by the device. In this state, all major functional blocks are disabled aside from a low power monitor on the nSLEEP pin and the powered off braking

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function if enabled. Passive gate pull downs are provided for the external MOSFET gates to maintain the MOSFETs in an off state. After exiting the inactive sleep state, all device registers will be reset to defaults.

7.4.2 Standby State

When the nSLEEP pin is logic high and DVDD input has crossed the V_{DVDD_POR} threshold, the device enters a power on standby state after t_{WAKE} delay. The digital core and SPI communication will be active but the charge pump and gate drivers will remain disabled until the PVDD input has crossed the V_{PVDD_UV} threshold. In this state, the SPI registers can be programmed and faults reported, but no gate driver operation is possible.

7.4.3 Operating State

When the nSLEEP pin is logic high, the DVDD input has crossed the V_{DVDD_POR} threshold, and the PVDD input has crossed the V_{PVDD_UV} threshold, the devices enters its full operating state. In this state, all major functional blocks are active aside from the gate drivers. The gate drivers must be enabled through the EN_DRV register bit before full operation can begin.

On H/W device variants, the device will automatically enable the drivers in the operating state.

7.5 Programming

7.5.1 SPI Interface

An SPI bus is used to set device configurations, operating parameters, and read out diagnostic information on the DRV871x-Q1 devices. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16 bit word, with an 8 bit command and 8 bits of data. The SPI output data (SDO) word consists of the fault status indication bits and then the register data being accessed for read commands or null for write commands. The data sequence between the MCU and the SPI slave driver is shown in Figure 7-30.

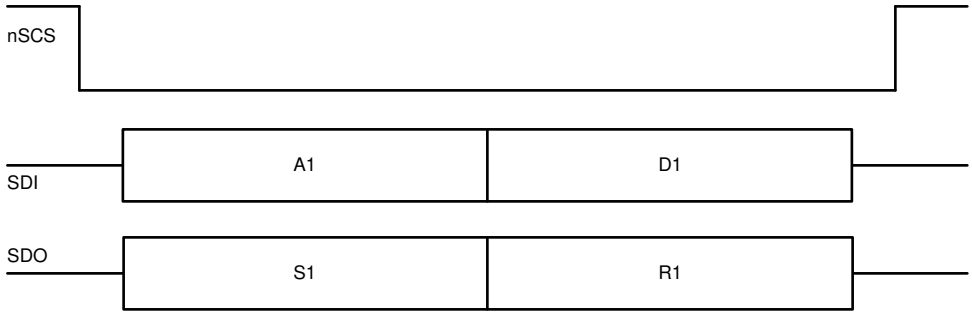

Figure 7-30. SPI Data Frame

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error (SCLK_FLT) occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin follow the 8 bit command data.

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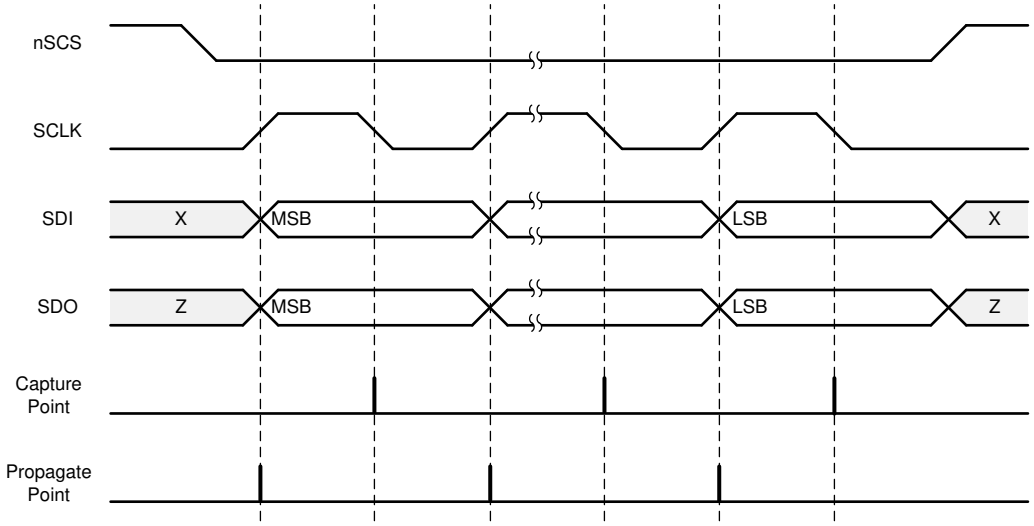

Figure 7-31. SPI Slave Timing Diagram

7.5.2 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B14)
- 6 address bits, A (bits B13 through B8)
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 8 bits makes up the IC status register. The report word is the content of the register being accessed.

For a write command (W0 = 0), the response word consists of the fault status indication bits followed by the existing data in the register being written to.

For a read command (W0 = 1), the response word consists of the fault status indications bits followed by the data currently in the register being read.

Table 7-18. SDI Input Data Word Format

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 7-19. SDO Output Data Word Format

	IC Status								Report							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	FAULT	WARN	DS_GS	UV	OV	OT_WD_AGD	D7	D6	D5	D4	D3	D2	D1	D0

7.5.3 SPI Interface for Multiple Slaves

Multiple DRV871x-Q1 devices can be connected to the master controller with and without the daisy chain. For connecting a 'n' number of DRV871x-Q1 to a master controller without using a daisy chain, 'n' number of I/O resources from master controller has to utilized for nSCS pins as shown Figure 7-32. Whereas, if the daisy chain configuration is used, then a single nSCS line can be used for connecting multiple DRV871x-Q1 devices. Figure 7-33

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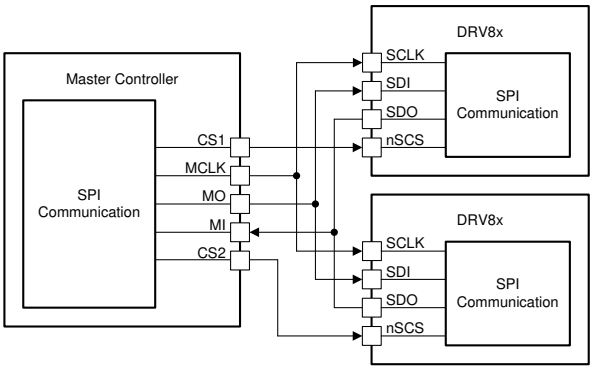

Figure 7-32. SPI Operation Without Daisy Chain

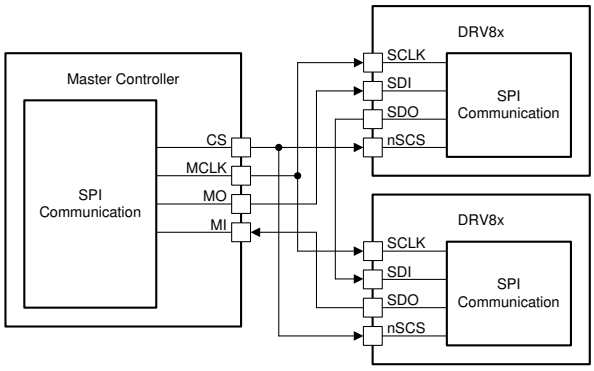

Figure 7-33. SPI Operation With Daisy Chain

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7.5.3.1 SPI Interface for Multiple Slaves in Daisy Chain

The DRV871x-Q1 device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU. Figure 7-34 shows the topology when 3 devices are connected in series with waveforms.

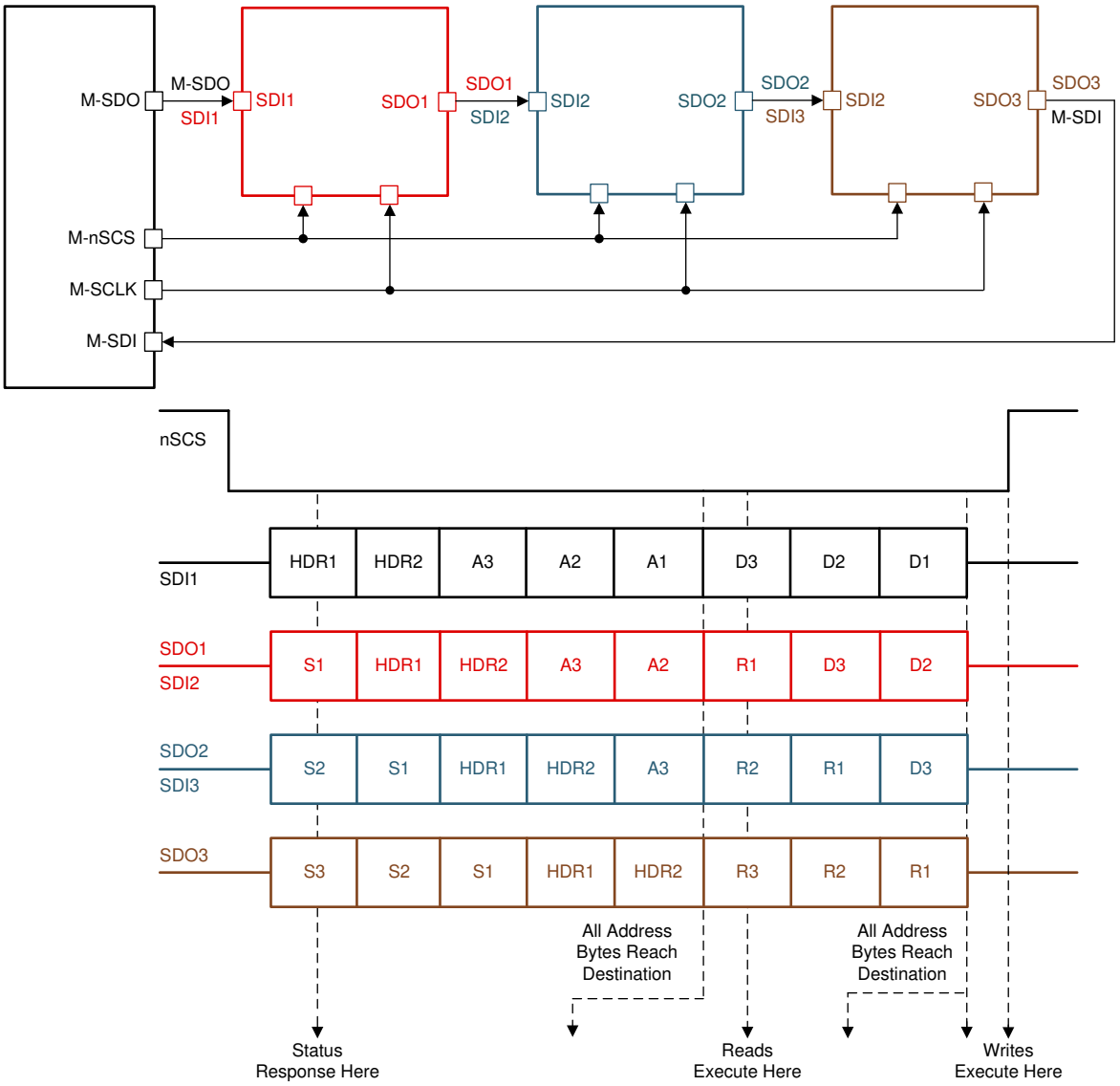

Figure 7-34. Daisy Chain SPI Operation

The first device in the chain shown above receives data from the master controller in the following format. See SDI1 in Figure 7-34

- 2 bytes of Header
- 3 bytes of Address
- 3 bytes of Data

After the data has been transmitted through the chain, the master controller receives it in the following format. See SDO3 in Figure 7-34

- 3 bytes of Status

- 2 bytes of Header (should be identical to the information controller sent)
- 3 bytes of Report

The Header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. N5 through N0 are 6 bits dedicated to show the number of device in the chain as shown in Figure 7-35. Up to 63 devices can be connected in series per daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

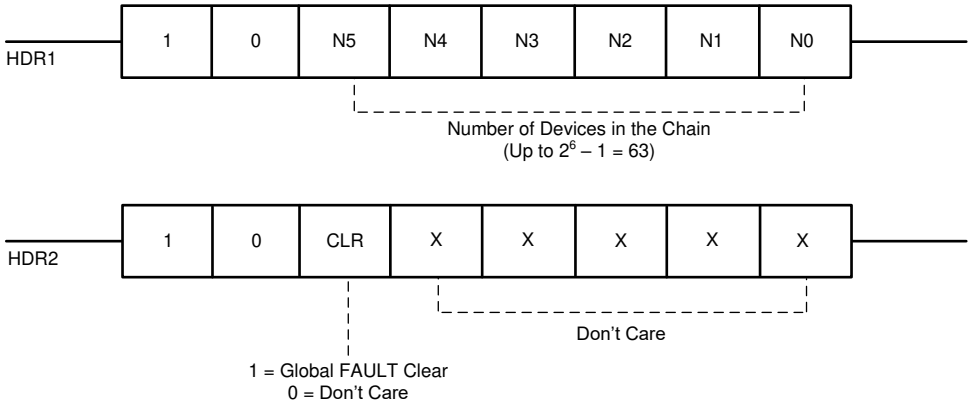

Figure 7-35. Header Bits

The Status byte provides information about the fault status register for each device in the daisy chain as shown in Figure 7-36. That way the master controller does not have to initiate a read command to read the fault status from any particular device. This saves the controller additional read commands and makes the system more efficient to determine fault conditions flagged in a device.

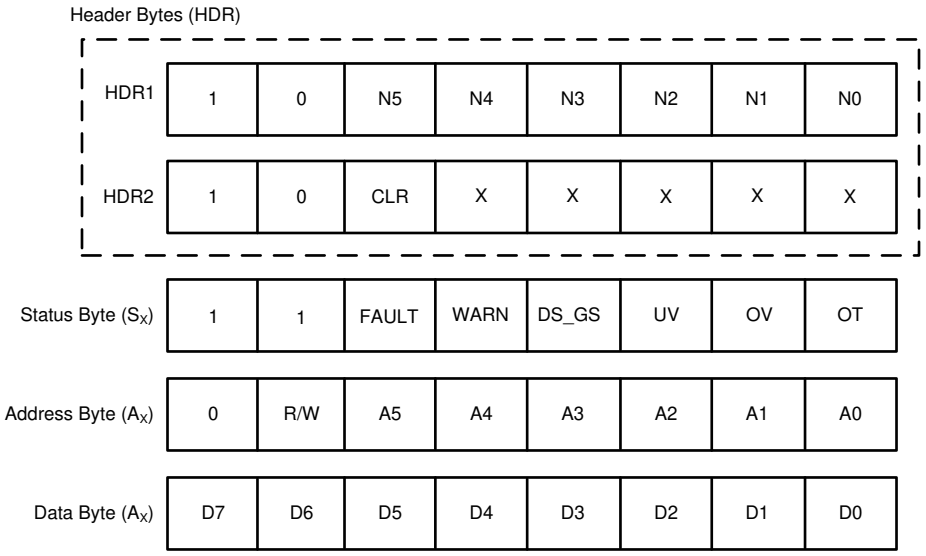

Figure 7-36. Daisy Chain Read Registers

When data passes through a device, it determines the position of itself in the chain by counting the number of Status bytes it receives following by the first Header byte. For example, in this 3 device configuration, device 2 in the chain will receive two Status bytes before receiving HDR1 byte, followed by HDR2 byte.

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From the two Status bytes it knows that its position is second in the chain, and from HDR2 byte it knows how many devices are connected in the chain. That way it only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a single device connection. The Report bytes (R1 through R3), as shown in the figure above, is the content of the register being accessed.

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8 Register Maps

The DRV8718-Q1 and DRV8714-Q1 registers provide variety of feedback information and configuration options. These include specific fault diagnostics, general device configurations, driver configurations, fault and diagnostic configurations, and amplifier configurations. Additionally, the advanced register maps provide advanced driver functions to assist in certain system conditions, but not required for standard operation of the device.

To assist with software development and reuse, the DRV8718-Q1 and DRV8714-Q1 register maps share an overlapping register structure with differences for specific device properties. The primary differences between the two device register maps are outlined below.

Register Map Differences:

- DRV8714-Q1: VDS_STAT2 (02h) and VGS_STAT2 (04h) are reserved.
- DRV8714-Q1: BRG_CTRL2 (0Ah) and PWM_CTRL2 (0Ch) are repurposed for H-bridge control functions.
- DRV8714-Q1: PWM_CTRL3 [3:0] (0Dh) PWM_CTRL4 [3:0] (0Eh) are reserved.
- DRV8714-Q1: IDRV_CTRL5, 6, 7, and 8 (13h, 14h, 15h, and 16h) are reserved.
- DRV8714-Q1: IDRV_CTRL9 [3:0] (17h) are reserved.
- DRV8714-Q1: DRV_CTRL2, 3, 4, 5, and 6 (19h, 1Ah, 1Bh, 1Ch, and 1Dh) are now half-bridge specific instead of H-bridge specific (DRV8718-Q1).
- DRV8714-Q1: VDS_CTRL3 (21h) and VDS_CTRL4 (22h) are reserved.
- DRV8714-Q1: OLSC_CTRL2 (24h) is reserved.

Advanced Register Map Differences:

- DRV8714-Q1: All register are now half-bridge specific instead of H-bridge specific (DRV8718-Q1).

Note

The DRV8718-Q1 56-Pin VQFN (RVJ) and DRV8714-Q1 56-Pin VQFN (RVJ) packages are drop in pin-to-pin compatible. Please note that the locations of half-bridges 1,2,3 and 4 will be shifted for the DRV8714-Q1 to help with PCB routing.

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8.1 DRV8718-Q1 Register Map

Table 8-1 lists the memory-mapped registers for the DRV8718-Q1. All register addresses not listed should be considered as reserved locations and the register contents should not be modified. Descriptions of reserved locations are provided for reference only.

Table 8-1. DRV8718-Q1 Register Map

Name	7	6	5	4	3	2	1	0	Type	Addr
IC_STAT1	SPI_OK	POR	FAULT	WARN	DS_GS	UV	OV	OT_WD_AGD	R	00h
VDS_STAT1	VDS_H1	VDS_L1	VDS_H2	VDS_L2	VDS_H3	VDS_L3	VDS_H4	VDS_L4	R	01h
VDS_STAT2	VDS_H5	VDS_L5	VDS_H6	VDS_L6	VDS_H7	VDS_L7	VDS_H8	VDS_L8	R	02h
VGS_STAT1	VGS_H1	VGS_L1	VGS_H2	VGS_L2	VGS_H3	VGS_L3	VGS_H4	VGS_L4	R	03h
VGS_STAT2	VGS_H5	VGS_L5	VGS_H6	VGS_L6	VGS_H7	VGS_L7	VGS_H8	VGS_L8	R	04h
IC_STAT2	PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	WD_FLT	SCLK_FLT	RSVD	R	05h
IC_STAT3	RSVD				IC_ID				R	06h
IC_CTRL1	EN_DRV	EN_OLSC	RSVD		LOCK			CLR_FLT	R/W	07h
IC_CTRL2	DIS_SSC	DRVOFF_nFLT	CP_MODE		WD_EN	WD_FLT_M	WD_WIN	WD_RST	R/W	08h
BRG_CTRL1	HB1_CTRL		HB2_CTRL		HB3_CTRL		HB4_CTRL		R/W	09h
BRG_CTRL2	HB5_CTRL		HB6_CTRL		HB7_CTRL		HB8_CTRL		R/W	0Ah
PWM_CTRL1	HB1_PWM		HB2_PWM		HB3_PWM		HB4_PWM		R/W	0Bh
PWM_CTRL2	HB5_PWM		HB6_PWM		HB7_PWM		HB8_PWM		R/W	0Ch
PWM_CTRL3	HB1_HL	HB2_HL	HB3_HL	HB4_HL	HB5_HL	HB6_HL	HB7_HL	HB8_HL	R/W	0Dh
PWM_CTRL4	HB1_FW	HB2_FW	HB3_FW	HB4_FW	HB5_FW	HB6_FW	HB7_FW	HB8_FW	R/W	0Eh
IDRV_CTRL1	IDRVP_1				IDRVN_1				R/W	0Fh
IDRV_CTRL2	IDRVP_2				IDRVN_2				R/W	10h
IDRV_CTRL3	IDRVP_3				IDRVN_3				R/W	11h
IDRV_CTRL4	IDRVP_4				IDRVN_4				R/W	12h
IDRV_CTRL5	IDRVP_5				IDRVN_5				R/W	13h
IDRV_CTRL6	IDRVP_6				IDRVN_6				R/W	14h
IDRV_CTRL7	IDRVP_7				IDRVN_7				R/W	15h
IDRV_CTRL8	IDRVP_8				IDRVN_8				R/W	16h
IDRV_CTRL9	IDRV_LO1	IDRV_LO2	IDRV_LO3	IDRV_LO4	IDRV_LO5	IDRV_LO6	IDRV_LO7	IDRV_LO8	R/W	17h
DRV_CTRL1	VGS_MODE		VGS_IND	VGS_LVL	VGS_HS_DIS	VDS_MODE		VDS_IND	R/W	18h
DRV_CTRL2	RSVD		VGS_TDRV_12			VGS_TDRV_34			R/W	19h
DRV_CTRL3	RSVD		VGS_TDRV_56			VGS_TDRV_78			R/W	1Ah
DRV_CTRL4	VGS_TDEAD_12		VGS_TDEAD_34		VGS_TDEAD_56		VGS_TDEAD_78		R/W	1Bh
DRV_CTRL5	VDS_DG_12		VDS_DG_34		VDS_DG_56		VDS_DG_78		R/W	1Ch
DRV_CTRL6	VDS_IDRVN_12		VDS_IDRVN_34		VDS_IDRVN_56		VDS_IDRVN_78		R/W	1Dh
DRV_CTRL7	RSVD								R/W	1Eh
VDS_CTRL1	VDS_LVL_1				VDS_LVL_2				R/W	1Fh
VDS_CTRL2	VDS_LVL_3				VDS_LVL_4				R/W	20h
VDS_CTRL3	VDS_LVL_5				VDS_LVL_6				R/W	21h
VDS_CTRL4	VDS_LVL_7				VDS_LVL_8				R/W	22h
OLSC_CTRL1	PU_SH_1	PD_SH_1	PU_SH_2	PD_SH_2	PU_SH_3	PD_SH_3	PU_SH_4	PD_SH_4	R/W	23h
OLSC_CTRL2	PU_SH_5	PD_SH_5	PU_SH_6	PD_SH_6	PU_SH_7	PD_SH_7	PU_SH_8	PD_SH_8	R/W	24h
UVOV_CTRL	PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_DG		PVDD_OV_LVL	VCP_UV_MODE	VCP_UV_LVL	R/W	25h
CSA_CTRL1	RSVD		CSA_DIV_1	CSA_GAIN_1		CSA_DIV_2	CSA_GAIN_2		R/W	26h
CSA_CTRL2	RSVD		CSA_BLK_SEL_1			CSA_BLK_1			R/W	27h
CSA_CTRL3	RSVD		CSA_BLK_SEL_2			CSA_BLK_2			R/W	28h
RSVD_CTRL	RSVD								R/W	29h

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Table 8-2 provides advanced control functions described in the Propagation Delay Reduction (PDR), Duty Cycle Compensation (DCC), and Slew Time Control (STC) sections. These are not necessary for typical use cases of the DRV871x-Q1 and may be utilized as needed to meet specific system requirements.

Table 8-2. DRV8718-Q1 Advanced Function Register Map

Name	7	6	5	4	3	2	1	0	Type	Addr
AGD_CTRL1	AGD_THR		AGD_ISTRONG		SET_AGD_12	SET_AGD_34	SET_AGD_56	SET_AGD_78	R/W	2Ah
PDR_CTRL1	PRE_MAX_12		T_DON_DOFF_12						R/W	2Bh
PDR_CTRL2	PRE_MAX_34		T_DON_DOFF_34						R/W	2Ch
PDR_CTRL3	PRE_MAX_56		T_DON_DOFF_56						R/W	2Dh
PDR_CTRL4	PRE_MAX_78		T_DON_DOFF_78						R/W	2Eh
PDR_CTRL5	T_PRE_CHR_12		T_PRE_DCHR_12		PRE_CHR_INIT_12		PRE_DCHR_INIT_12		R/W	2Fh
PDR_CTRL6	T_PRE_CHR_34		T_PRE_DCHR_34		PRE_CHR_INIT_34		PRE_DCHR_INIT_34		R/W	30h
PDR_CTRL7	T_PRE_CHR_56		T_PRE_DCHR_56		PRE_CHR_INIT_56		PRE_DCHR_INIT_56		R/W	31h
PDR_CTRL8	T_PRE_CHR_78		T_PRE_DCHR_78		PRE_CHR_INIT_78		PRE_DCHR_INIT_78		R/W	32h
PDR_CTRL9	EN_PDR_12	RSVD	KP_PDR_12		EN_PDR_34	RSVD	KP_PDR_34		R/W	33h
PDR_CTRL10	EN_PDR_56	RSVD	KP_PDR_56		EN_PDR_78	RSVD	KP_PDR_78		R/W	34h
STC_CTRL1	T_RISE_FALL_12				EN_STC_12	STC_ERR_12	KP_STC_12		R/W	35h
STC_CTRL2	T_RISE_FALL_34				EN_STC_34	STC_ERR_34	KP_STC_34		R/W	36h
STC_CTRL3	T_RISE_FALL_56				EN_STC_56	STC_ERR_56	KP_STC_56		R/W	37h
STC_CTRL4	T_RISE_FALL_78				EN_STC_78	STC_ERR_78	KP_STC_78		R/W	38h
DCC_CTRL1	EN_DCC_12	EN_DCC_34	EN_DCC_56	EN_DCC_78	IDIR_MAN_12	IDIR_MAN_34	IDIR_MAN_56	IDIR_MAN_78	R/W	39h
PST_CTRL1	FW_MAX_12	FW_MAX_34	FW_MAX_56	FW_MAX_78	EN_PST_DLY_12	EN_PST_DLY_34	EN_PST_DLY_56	EN_PST_DLY_78	R/W	3Ah
PST_CTRL2	KP_PST_12		KP_PST_34		KP_PST_56		KP_PST_78		R/W	3Bh
SGD_STAT1	IDIR_12	IDIR_34	IDIR_56	IDIR_78	IDIR_WARN_12	IDIR_WARN_34	IDIR_WARN_56	IDIR_WARN_78	R	3Ch
SGD_STAT2	PCHR_WARN_12	PCHR_WARN_34	PCHR_WARN_56	PCHR_WARN_12	PDCHR_WARN_12	PDCHR_WARN_12	PDCHR_WARN_12	PDCHR_WARN_12	R	3Dh
SGD_STAT3	STC_WARN_F_12	STC_WARN_F_34	STC_WARN_F_56	STC_WARN_F_78	STC_WARN_R_12	STC_WARN_R_34	STC_WARN_R_56	STC_WARN_R_78	R	3Eh

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8.2 DRV8714-Q1 Register Map

DRV8714-Q1 Register Map lists the memory-mapped registers for the DRV8714-Q1. All register addresses not listed should be considered as reserved locations and the register contents should not be modified. Descriptions of reserved locations are provided for reference only.

Table 8-3. DRV8714-Q1 Register Map

Name	7	6	5	4	3	2	1	0	Type	Addr.
IC_STAT1	SPI_OK	POR	FAULT	WARN	DS_GS	UV	OV	OT_WD_AGD	R	00h
VDS_STAT1	VDS_H1	VDS_L1	VDS_H2	VDS_L2	VDS_H3	VDS_L3	VDS_H4	VDS_L4	R	01h
VDS_STAT2	RSVD								R	02h
VGS_STAT1	VGS_H1	VGS_L1	VGS_H2	VGS_L2	VGS_H3	VGS_L3	VGS_H4	VGS_L4	R	03h
VGS_STAT2	RSVD								R	04h
IC_STAT2	PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	WD_FLT	SCLK_FLT	RSVD	R	05h
IC_STAT3	RSVD				IC_ID				R	06h
IC_CTRL1	EN_DRV	EN_OLSC	BRG_MODE		LOCK			CLR_FLT	R/W	07h
IC_CTRL2	DIS_SSC	DRVOFF_nFLT	CP_MODE		WD_EN	WD_FLT_M	WD_WIN	WD_RST	R/W	08h
BRG_CTRL1	HB1_CTRL		HB2_CTRL		HB3_CTRL		HB4_CTRL		R/W	09h
BRG_CTRL2	S_IN1/EN1	S_IN2/PH1	HIZ1	RSVD	S_IN3/EN2	S_IN4/PH2	HIZ2	RSVD	R/W	0Ah
PWM_CTRL1	HB1_PWM		HB2_PWM		HB3_PWM		HB4_PWM		R/W	0Bh
PWM_CTRL2	IN1/EN1_MODE	IN2/PH1_MODE	FW1	RSVD	IN3/EN2_MODE	IN4/PH2_MODE	FW2	RSVD	R/W	0Ch
PWM_CTRL3	HB1_HL	HB2_HL	HB3_HL	HB4_HL	RSVD				R/W	0Dh
PWM_CTRL4	HB1_FW	HB2_FW	HB3_FW	HB4_FW	RSVD				R/W	0Eh
IDRV_CTRL1	IDRVP_1				IDRVN_1				R/W	0Fh
IDRV_CTRL2	IDRVP_2				IDRVN_2				R/W	10h
IDRV_CTRL3	IDRVP_3				IDRVN_3				R/W	11h
IDRV_CTRL4	IDRVP_4				IDRVN_4				R/W	12h
IDRV_CTRL5	RSVD								R/W	13h
IDRV_CTRL6	RSVD								R/W	14h
IDRV_CTRL7	RSVD								R/W	15h
IDRV_CTRL8	RSVD								R/W	16h
IDRV_CTRL9	IDRV_LO1	IDRV_LO2	IDRV_LO3	IDRV_LO4	RSVD				R/W	17h
DRV_CTRL1	VGS_MODE		VGS_IND	VGS_LVL	VGS_HS_DIS	VDS_MODE		VDS_IND	R/W	18h
DRV_CTRL2	RSVD		VGS_TDRV_1			VGS_TDRV_2			R/W	19h
DRV_CTRL3	RSVD		VGS_TDRV_3			VGS_TDRV_4			R/W	1Ah
DRV_CTRL4	VGS_TDEAD_1		VGS_TDEAD_2		VGS_TDEAD_3		VGS_TDEAD_4		R/W	1Bh
DRV_CTRL5	VDS_DG_1		VDS_DG_2		VDS_DG_3		VDS_DG_4		R/W	1Ch
DRV_CTRL6	VDS_IDRVN_1		VDS_IDRVN_2		VDS_IDRVN_3		VDS_IDRVN_4		R/W	1Dh
DRV_CTRL7	RSVD								R/W	1Eh
VDS_CTRL1	VDS_LVL_1				VDS_LVL_2				R/W	1Fh
VDS_CTRL2	VDS_LVL_3				VDS_LVL_4				R/W	20h
VDS_CTRL3	RSVD								R/W	21h
VDS_CTRL4	RSVD								R/W	22h
OLSC_CTRL1	PU_SH_1	PD_SH_1	PU_SH_2	PD_SH_2	PU_SH_3	PD_SH_3	PU_SH_4	PD_SH_4	R/W	23h
OLSC_CTRL2	RSVD								R/W	24h
UVOV_CTRL	PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_DG		PVDD_OV_LVL	VCP_UV_MODE	VCP_UV_LVL	R/W	25h
CSA_CTRL1	RSVD		CSA_DIV_1	CSA_GAIN_1		CSA_DIV_2	CSA_GAIN_2		R/W	26h
CSA_CTRL2	RSVD		CSA_BLK_SEL_1			CSA_BLK_1			R/W	27h
CSA_CTRL3	RSVD		CSA_BLK_SEL_2			CSA_BLK_2			R/W	28h
RSVD_CTRL	RSVD								R/W	29h

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DRV8714-Q1 Advanced Function Register Map provides advanced control functions described in the Propagation Delay Reduction (PDR), Duty Cycle Compensation (DCC), and Slew Time Control (STC) sections. These are not necessary for typical use cases of the DRV871x-Q1 and may be utilized as needed to meet specific system requirements.

Table 8-4. DRV8714-Q1 Advanced Function Register Map

Name	7	6	5	4	3	2	1	0	Type	Addr.
AGD_CTRL1	AGD_THR		AGD_ISTRONG		RSVD				R/W	2Ah
PDR_CTRL1	PRE_MAX_1		T_DON_DOFF_1						R/W	2Bh
PDR_CTRL2	PRE_MAX_2		T_DON_DOFF_2						R/W	2Ch
PDR_CTRL3	PRE_MAX_3		T_DON_DOFF_3						R/W	2Dh
PDR_CTRL4	PRE_MAX_4		T_DON_DOFF_4						R/W	2Eh
PDR_CTRL5	T_PRE_CHR_1		T_PRE_DCHR_1		PRE_CHR_INIT_1		PRE_DCHR_INIT_1		R/W	2Fh
PDR_CTRL6	T_PRE_CHR_2		T_PRE_DCHR_2		PRE_CHR_INIT_2		PRE_DCHR_INIT_2		R/W	30h
PDR_CTRL7	T_PRE_CHR_3		T_PRE_DCHR_3		PRE_CHR_INIT_3		PRE_DCHR_INIT_3		R/W	31h
PDR_CTRL8	T_PRE_CHR_4		T_PRE_DCHR_4		PRE_CHR_INIT_4		PRE_DCHR_INIT_4		R/W	32h
PDR_CTRL9	EN_PDR_1	RSVD	KP_PDR_1		EN_PDR_2	RSVD	KP_PDR_2		R/W	33h
PDR_CTRL10	EN_PDR_3	RSVD	KP_PDR_3		EN_PDR_4	RSVD	KP_PDR_4		R/W	34h
STC_CTRL1	T_RISE_FALL_1				EN_STC_1	STC_ERR_1	KP_STC_1		R/W	35h
STC_CTRL2	T_RISE_FALL_2				EN_STC_2	STC_ERR_2	KP_STC_2		R/W	36h
STC_CTRL3	T_RISE_FALL_3				EN_STC_3	STC_ERR_3	KP_STC_3		R/W	37h
STC_CTRL4	T_RISE_FALL_4				EN_STC_4	STC_ERR_4	KP_STC_4		R/W	38h
DCC_CTRL1	EN_DCC_1	EN_DCC_2	EN_DCC_3	EN_DCC_4	IDIR_MAN_1	IDIR_MAN_2	IDIR_MAN_3	IDIR_MAN_4	R/W	39h
PST_CTRL1	FW_MAX_1	FW_MAX_2	FW_MAX_3	FW_MAX_4	EN_PST_DLY_1	EN_PST_DLY_2	EN_PST_DLY_3	EN_PST_DLY_4	R/W	3Ah
PST_CTRL2	KP_PST_1		KP_PST_2		KP_PST_3		KP_PST_4		R/W	3Bh
SGD_STAT1	IDIR_1	IDIR_2	IDIR_3	IDIR_4	IDIR_WARN_1	IDIR_WARN_2	IDIR_WARN_3	IDIR_WARN_4	R	3Ch
SGD_STAT2	PCHR_WARN_1	PCHR_WARN_2	PCHR_WARN_3	PCHR_WARN_4	PDCHR_WARN_1	PDCHR_WARN_2	PDCHR_WARN_3	PDCHR_WARN_4	R	3Dh
SGD_STAT3	STC_WARN_F_1	STC_WARN_F_2	STC_WARN_F_3	STC_WARN_F_4	STC_WARN_R_1	STC_WARN_R_2	STC_WARN_R_3	STC_WARN_R_4	R	3Eh

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8.3 DRV8718-Q1 Register Descriptions

8.3.1 DRV8718-Q1_STATUS Registers

Table 8-5 lists the DRV8718-Q1_STATUS registers. All register offset addresses not listed in Table 8-5 should be considered as reserved locations and the register contents should not be modified.

Table 8-5. DRV8718-Q1_STATUS Registers

Address	Acronym	Register Name	Section
0h	IC_STAT1	Global fault and warning status indicators	Go
1h	VDS_STAT1	Half-bridge 1-4 VDS overcurrent fault status indicators	Go
2h	VDS_STAT2	Half-bridge 5-8 VDS overcurrent fault status indicators	Go
3h	VGS_STAT1	Half-bridge 1-4 VGS gate fault status indicators	Go
4h	VGS_STAT2	Half-bridge 5-8 VGS gate fault status indicators	Go
5h	IC_STAT2	Voltage, temperature and interface fault status indicators	Go
6h	IC_STAT3	Device variant ID status register	Go

Complex bit access types are encoded to fit into small table cells. Table 8-6 shows the codes that are used for access types in this section.

Table 8-6. DRV8718-Q1_STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
- *n*		Value after reset or the default value

8.3.1.1 IC_STAT1 Register (Address = 0h) [Reset = C0h]

IC_STAT1 is shown in Figure 8-1 and described in Table 8-7.

Return to the Summary Table.

Status register for global fault and warning indicators. Detailed fault information is available in remaining status registers.

Figure 8-1. IC_STAT1 Register

7	6	5	4	3	2	1	0
SPI_OK	POR	FAULT	WARN	DS_GS	UV	OV	OT_WD_AGD
R-1b	R-1b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-7. IC_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_OK	R	1b	Indicates if a SPI communications fault has been detected. 0b = One or multiple of SCLK_FLT in the prior frames. 1b = No SPI fault has been detected
6	POR	R	1b	Indicates power-on-reset condition. 0b = No power-on-reset condition detected. 1b = Power-on reset condition detected.
5	FAULT	R	0b	Fault indicator. Mirrors nFAULT pin.
4	WARN	R	0b	Warning indicator.
3	DS_GS	R	0b	Logic OR of VDS and VGS fault indicators.
2	UV	R	0b	Undervoltage indicator.
1	OV	R	0b	Overvoltage indicator.

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Table 8-7. IC_STAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OT_WD_AGD	R	0b	Logic OR of OTW, OTSD, WD_FLT, IDIR_WARN, PCHR_WARN, PDCHR_WARN, and STC_WARN indicators.

8.3.1.2 VDS_STAT1 Register (Address = 1h) [Reset = 0h]

VDS_STAT1 is shown in Figure 8-2 and described in Table 8-8.

Return to the Summary Table.

Status register for the specific MOSFET VDS overcurrent fault indication for half-bridges 1-4.

Figure 8-2. VDS_STAT1 Register

7	6	5	4	3	2	1	0
VDS_H1	VDS_L1	VDS_H2	VDS_L2	VDS_H3	VDS_L3	VDS_H4	VDS_L4
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-8. VDS_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VDS_H1	R	0b	Indicates VDS overcurrent fault on the high-side 1 MOSFET.
6	VDS_L1	R	0b	Indicates VDS overcurrent fault on the low-side 1 MOSFET.
5	VDS_H2	R	0b	Indicates VDS overcurrent fault on the high-side 2 MOSFET.
4	VDS_L2	R	0b	Indicates VDS overcurrent fault on the low-side 2 MOSFET.
3	VDS_H3	R	0b	Indicates VDS overcurrent fault on the high-side 3 MOSFET.
2	VDS_L3	R	0b	Indicates VDS overcurrent fault on the low-side 3 MOSFET.
1	VDS_H4	R	0b	Indicates VDS overcurrent fault on the high-side 4 MOSFET.
0	VDS_L4	R	0b	Indicates VDS overcurrent fault on the low-side 4 MOSFET.

8.3.1.3 VDS_STAT2 Register (Address = 2h) [Reset = 0h]

VDS_STAT2 is shown in Figure 8-3 and described in Table 8-9.

Return to the Summary Table.

Status register for the specific MOSFET VDS overcurrent fault indication for half-bridges 5-8.

Figure 8-3. VDS_STAT2 Register

7	6	5	4	3	2	1	0
VDS_H5	VDS_L5	VDS_H6	VDS_L6	VDS_H7	VDS_L7	VDS_H8	VDS_L8
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-9. VDS_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VDS_H5	R	0b	Indicates VDS overcurrent fault on the high-side 5 MOSFET.
6	VDS_L5	R	0b	Indicates VDS overcurrent fault on the low-side 5 MOSFET.
5	VDS_H6	R	0b	Indicates VDS overcurrent fault on the high-side 6 MOSFET.
4	VDS_L6	R	0b	Indicates VDS overcurrent fault on the low-side 6 MOSFET.
3	VDS_H7	R	0b	Indicates VDS overcurrent fault on the high-side 7 MOSFET.
2	VDS_L7	R	0b	Indicates VDS overcurrent fault on the low-side 7 MOSFET.
1	VDS_H8	R	0b	Indicates VDS overcurrent fault on the high-side 8 MOSFET.
0	VDS_L8	R	0b	Indicates VDS overcurrent fault on the low-side 8 MOSFET.

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8.3.1.4 VGS_STAT1 Register (Address = 3h) [Reset = 0h]

VGS_STAT1 is shown in Figure 8-4 and described in Table 8-10.

Return to the Summary Table.

Status register for the specific MOSFET VGS gate fault indication for half-bridges 1-4.

Figure 8-4. VGS_STAT1 Register

7	6	5	4	3	2	1	0
VGS_H1	VGS_L1	VGS_H2	VGS_L2	VGS_H3	VGS_L3	VGS_H4	VGS_L4
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-10. VGS_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VGS_H1	R	0b	Indicates VGS gate fault on the high-side 1 MOSFET.
6	VGS_L1	R	0b	Indicates VGS gate fault on the low-side 1 MOSFET.
5	VGS_H2	R	0b	Indicates VGS gate fault on the high-side 2 MOSFET.
4	VGS_L2	R	0b	Indicates VGS gate fault on the low-side 2 MOSFET.
3	VGS_H3	R	0b	Indicates VGS gate fault on the high-side 3 MOSFET.
2	VGS_L3	R	0b	Indicates VGS gate fault on the low-side 3 MOSFET.
1	VGS_H4	R	0b	Indicates VGS gate fault on the high-side 4 MOSFET.
0	VGS_L4	R	0b	Indicates VGS gate fault on the low-side 4 MOSFET.

8.3.1.5 VGS_STAT2 Register (Address = 4h) [Reset = 0h]

VGS_STAT2 is shown in Figure 8-5 and described in Table 8-11.

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Status register for the specific MOSFET VGS gate fault indication for half-bridges 5-8.

Figure 8-5. VGS_STAT2 Register

7	6	5	4	3	2	1	0
VGS_H5	VGS_L5	VGS_H6	VGS_L6	VGS_H7	VGS_L7	VGS_H8	VGS_L8
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-11. VGS_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VGS_H5	R	0b	Indicates VGS gate fault on the high-side 5 MOSFET.
6	VGS_L5	R	0b	Indicates VGS gate fault on the low-side 5 MOSFET.
5	VGS_H6	R	0b	Indicates VGS gate fault on the high-side 6 MOSFET.
4	VGS_L6	R	0b	Indicates VGS gate fault on the low-side 6 MOSFET.
3	VGS_H7	R	0b	Indicates VGS gate fault on the high-side 7 MOSFET.
2	VGS_L7	R	0b	Indicates VGS gate fault on the low-side 7 MOSFET.
1	VGS_H8	R	0b	Indicates VGS gate fault on the high-side 8 MOSFET.
0	VGS_L8	R	0b	Indicates VGS gate fault on the low-side 8 MOSFET.

8.3.1.6 IC_STAT2 Register (Address = 5h) [Reset = 0h]

IC_STAT2 is shown in Figure 8-6 and described in Table 8-12.

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Status register for specific undervoltage, overvoltage, overtemperature, and interface fault indications.

Figure 8-6. IC_STAT2 Register

7	6	5	4	3	2	1	0
PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	WD_FLT	SCLK_FLT	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-12. IC_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_UV	R	0b	Indicates undervoltage fault on PVDD pin.
6	PVDD_OV	R	0b	Indicates overvoltage fault on PVDD pin.
5	VCP_UV	R	0b	Indicates undervoltage fault on VCP pin.
4	OTW	R	0b	Indicates overtemperature warning.
3	OTSD	R	0b	Indicates overtemperature shutdown.
2	WD_FLT	R	0b	Indicated watchdog timer fault.
1	SCLK_FLT	R	0b	Indicates SPI clock (frame) fault when the number of SCLK pulses in a transaction frame are not equal to 16. Not reported on FAULT or nFAULT pin.
0	RESERVED	R	0b	Reserved

8.3.1.7 IC_STAT3 Register (Address = 6h) [Reset = 8h]

IC_STAT3 is shown in Figure 8-7 and described in Table 8-13.

Return to the Summary Table.

Status register with device ID for either DRV8718-Q1 or DRV8714-Q1.

Figure 8-7. IC_STAT3 Register

7	6	5	4	3	2	1	0
RESERVED				IC_ID			
R-0000b				R-1000b			

Table 8-13. IC_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved
3-0	IC_ID	R	1000b	Device identification field. 0100b = DRV8714-Q1, 4 half-bridge gate driver. 1000b = DRV8718-Q1, 8 half-bridge gate driver.

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8.3.2 DRV8718-Q1_CONTROL Registers

Table 8-14 lists the DRV8718-Q1_CONTROL registers. All register offset addresses not listed in Table 8-14 should be considered as reserved locations and the register contents should not be modified.

Table 8-14. DRV8718-Q1_CONTROL Registers

Address	Acronym	Register Name	Section
7h	IC_CTRL1	Device general function control register 1	Go
8h	IC_CTRL2	Device general function control register 2	Go
9h	BRG_CTRL1	Half-bridge 1-4 output state control	Go
Ah	BRG_CTRL2	Half-bridge 5-8 output state control	Go
Bh	PWM_CTRL1	Half-bridge 1-4 PWM mapping control	Go
Ch	PWM_CTRL2	Half-bridge 5-8 PWM mapping control	Go
Dh	PWM_CTRL3	Half-bridge 1-8 high-side or low-side drive control	Go
Eh	PWM_CTRL4	Half-bridge 1-8 freewheeling configuration	Go
Fh	IDRV_CTRL1	Half-bridge 1 gate drive source/sink current	Go
10h	IDRV_CTRL2	Half-bridge 2 gate drive source/sink current	Go
11h	IDRV_CTRL3	Half-bridge 3 gate drive source/sink current	Go
12h	IDRV_CTRL4	Half-bridge 4 gate drive source/sink current	Go
13h	IDRV_CTRL5	Half-bridge 5 gate drive source/sink current	Go
14h	IDRV_CTRL6	Half-bridge 6 gate drive source/sink current	Go
15h	IDRV_CTRL7	Half-bridge 7 gate drive source/sink current	Go
16h	IDRV_CTRL8	Half-bridge 8 gate drive source/sink current	Go
17h	IDRV_CTRL9	Half-bridge 1-8 gate drive low current control	Go
18h	DRV_CTRL1	Gate driver VGS and VDS monitor configuration	Go
19h	DRV_CTRL2	Half-bridge 1-4 VGS and VDS tDRV configuration	Go
1Ah	DRV_CTRL3	Half-bridge 5-8 VGS and VDS tDRV configuration	Go
1Bh	DRV_CTRL4	Half-bridge 1-8 VGS tDEAD_D configuration	Go
1Ch	DRV_CTRL5	Half-bridge 1-8 VDS tDS_DG configuration	Go
1Dh	DRV_CTRL6	Half-bridge 1-8 VDS fault pulldown current configuration	Go
1Fh	VDS_CTRL1	Half-bridge 1 and 2 VDS overcurrent threshold	Go
20h	VDS_CTRL2	Half-bridge 3 and 4 VDS overcurrent threshold	Go
21h	VDS_CTRL3	Half-bridge 5 and 6 VDS overcurrent threshold	Go
22h	VDS_CTRL4	Half-bridge 7 and 8 VDS overcurrent threshold	Go
23h	OLSC_CTRL1	Half-bridge 1-4 offline diagnostic control	Go
24h	OLSC_CTRL2	Half-bridge 5-8 offline diagnostic control	Go
25h	UVOV_CTRL	Undervoltage and overvoltage monitor configuration.	Go
26h	CSA_CTRL1	Shunt amplifier 1 and 2 configuration	Go
27h	CSA_CTRL2	Shunt amplifier 1 blanking configuration	Go
28h	CSA_CTRL3	Shunt amplifier 2 blanking configuration	Go

Complex bit access types are encoded to fit into small table cells. Table 8-15 shows the codes that are used for access types in this section.

Table 8-15. DRV8718-Q1_CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		

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Table 8-15. DRV8718-Q1_CONTROL Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
- *n*		Value after reset or the default value

8.3.2.1 IC_CTRL1 Register (Address = 7h) [Reset = 6h]

IC_CTRL1 is shown in Figure 8-8 and described in Table 8-16.

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Control register for driver and diagnostic enable, SPI lock, and clear fault command.

Figure 8-8. IC_CTRL1 Register

7	6	5	4	3	2	1	0
EN_DRV	EN_OLSC	RESERVED		LOCK			CLR_FLT
R/W-0b	R/W-0b	R-00b		R/W-011b			R/W-0b

Table 8-16. IC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_DRV	R/W	0b	Enable gate drivers. 0b = Gate driver output disabled and passive pulldowns enabled. 1b = Gate driver outputs enabled.
6	EN_OLSC	R/W	0b	Enable offline open load and short circuit diagnostic. 0b = Disabled. 1b = VDS monitors set into real-time voltage monitor mode and offline diagnostics current sources enabled.
5-4	RESERVED	R	00b	Reserved
3-1	LOCK	R/W	011b	Lock and unlock the control registers. Bit settings not listed have no effect. 011b = Unlock all control registers. 110b = Lock the control registers by ignoring further writes except to the LOCK register.
0	CLR_FLT	R/W	0b	Clear latched fault status information. 0b = Default state. 1b = Clear latched fault bits, resets to 0b after completion. Will also clear SPI fault and watchdog fault status.

8.3.2.2 IC_CTRL2 Register (Address = 8h) [Reset = 2h]

IC_CTRL2 is shown in Figure 8-9 and described in Table 8-17.

Return to the Summary Table.

Control register for pin mode, charge pump mode, and watchdog.

Figure 8-9. IC_CTRL2 Register

7	6	5	4	3	2	1	0
DIS_SSC	DRVOFF_nFLT	CP_MODE		WD_EN	WD_FLT_M	WD_WIN	WD_RST
R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-1b	R/W-0b

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Table 8-17. IC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_SSC	R/W	0b	Spread spectrum clocking 0b = Enabled. 1b = Disabled.
6	DRVOFF_nFLT	R/W	0b	Sets DRVOFF/nFLT multi-function pin mode. 0b = Pin functions as DRVOFF global driver disable. 1b = Pin functions as nFLT open-drain fault interrupt output.
5-4	CP_MODE	R/W	00b	Charge pump operating mode. 00b = Automatic switch between tripler and doubler mode. 01b = Always doubler mode. 10b = Always tripler mode. 11b = RSVD
3	WD_EN	R/W	0b	Watchdog timer enable. 0b = Watchdog timer disabled. 1b = Watchdog dog timer enabled.
2	WD_FLT_M	R/W	0b	Watchdog fault mode. Watchdog fault is cleared by CLR_FLT. 0b = Watchdog fault is reported to WD_FLT and WARN register bits. Gate drivers remain enabled and nFAULT is not asserted. 1b = Watchdog fault is reported to WD_FLT, FAULT register bits, and nFAULT pin. Gate drivers are disabled in response to watchdog fault.
1	WD_WIN	R/W	1b	Watchdog timer window. 0b = 4 to 40 ms 1b = 10 to 100 ms
0	WD_RST	R/W	0b	Watchdog restart. 0b by default after power up. Invert this bit to restart the watchdog timer. After written, the bit will reflect the new inverted value.

8.3.2.3 BRG_CTRL1 Register (Address = 9h) [Reset = 0h]

BRG_CTRL1 is shown in Figure 8-10 and described in Table 8-18.

Return to the Summary Table.

Control register to set the output state for half-bridges 1-4.

Figure 8-10. BRG_CTRL1 Register

7	6	5	4	3	2	1	0
HB1_CTRL		HB2_CTRL		HB3_CTRL		HB4_CTRL	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-18. BRG_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HB1_CTRL	R/W	00b	Half-bridge 1 output state control. 00b = High impedance (HI-Z). GH1 and GL1 pulldown. 01b = Drive low-side (LO). GH1 pulldown and GL1 pullup. 10b = Drive high-side (HI). GH1 pullup and GL1 pulldown. 11b = Input PWM control. HB1_PWM, HB1_HL, and HB1_FW.
5-4	HB2_CTRL	R/W	00b	Half-bridge 2 output state control. 00b = High impedance (HI-Z). GH2 and GL2 pulldown. 01b = Drive low-side (LO). GH2 pulldown and GL2 pullup. 10b = Drive high-side (HI). GH2 pullup and GL2 pulldown. 11b = Input PWM control. HB2_PWM, HB2_HL, and HB2_FW.
3-2	HB3_CTRL	R/W	00b	Half-bridge 3 output state control. 00b = High impedance (HI-Z). GH3 and GL3 pulldown. 01b = Drive low-side (LO). GH3 pulldown and GL3 pullup. 10b = Drive high-side (HI). GH3 pullup and GL3 pulldown. 11b = Input PWM control. HB3_PWM, HB3_HL, and HB3_FW.

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Table 8-18. BRG_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	HB4_CTRL	R/W	00b	Half-bridge 4 output state control. 00b = High impedance (HI-Z). GH4 and GL4 pulldown. 01b = Drive low-side (LO). GH4 pulldown and GL4 pullup. 10b = Drive high-side (HI). GH4 pullup and GL4 pulldown. 11b = Input PWM control. HB4_PWM, HB4_HL, and HB4_FW.

8.3.2.4 BRG_CTRL2 Register (Address = Ah) [Reset = 0h]

BRG_CTRL2 is shown in Figure 8-11 and described in Table 8-19.

Return to the Summary Table.

Control register to set the output state for half-bridges 5-8.

Figure 8-11. BRG_CTRL2 Register

7	6	5	4	3	2	1	0
HB5_CTRL		HB6_CTRL		HB7_CTRL		HB8_CTRL	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-19. BRG_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HB5_CTRL	R/W	00b	Half-bridge 5 output state control. 00b = High impedance (HI-Z). GH5 and GL5 pulldown. 01b = Drive low-side (LO). GH5 pulldown and GL5 pullup. 10b = Drive high-side (HI). GH5 pullup and GL5 pulldown. 11b = Input PWM control. HB5_PWM, HB5_HL, and HB5_FW.
5-4	HB6_CTRL	R/W	00b	Half-bridge 6 output state control. 00b = High impedance (HI-Z). GH6 and GL6 pulldown. 01b = Drive low-side (LO). GH6 pulldown and GL6 pullup. 10b = Drive high-side (HI). GH6 pullup and GL6 pulldown. 11b = Input PWM control. HB6_PWM, HB6_HL, and HB6_FW.
3-2	HB7_CTRL	R/W	00b	Half-bridge 7 output state control. 00b = High impedance (HI-Z). GH7 and GL7 pulldown. 01b = Drive low-side (LO). GH7 pulldown and GL7 pullup. 10b = Drive high-side (HI). GH7 pullup and GL7 pulldown. 11b = Input PWM control. HB7_PWM, HB7_HL, and HB7_FW.
1-0	HB8_CTRL	R/W	00b	Half-bridge 8 output state control. 00b = High impedance (HI-Z). GH8 and GL8 pulldown. 01b = Drive low-side (LO). GH8 pulldown and GL8 pullup. 10b = Drive high-side (HI). GH8 pullup and GL8 pulldown. 11b = Input PWM control. HB8_PWM, HB8_HL, and HB8_FW.

8.3.2.5 PWM_CTRL1 Register (Address = Bh) [Reset = 5h]

PWM_CTRL1 is shown in Figure 8-12 and described in Table 8-20.

Return to the Summary Table.

Control register to map the input PWM source for half-bridges 1-4.

Figure 8-12. PWM_CTRL1 Register

7	6	5	4	3	2	1	0
HB1_PWM		HB2_PWM		HB3_PWM		HB4_PWM	
R/W-00b		R/W-00b		R/W-01b		R/W-01b	

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Table 8-20. PWM_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HB1_PWM	R/W	00b	Configure PWM input source for half-bridge 1. 00b = IN1 01b = IN2 10b = IN3 11b = IN4
5-4	HB2_PWM	R/W	00b	Configure PWM input source for half-bridge 2. 00b = IN1 01b = IN2 10b = IN3 11b = IN4
3-2	HB3_PWM	R/W	01b	Configure PWM input source for half-bridge 3. 00b = IN1 01b = IN2 10b = IN3 11b = IN4
1-0	HB4_PWM	R/W	01b	Configure PWM input source for half-bridge 4. 00b = IN1 01b = IN2 10b = IN3 11b = IN4

8.3.2.6 PWM_CTRL2 Register (Address = Ch) [Reset = AFh]

PWM_CTRL2 is shown in Figure 8-13 and described in Table 8-21.

Return to the Summary Table.

Control register to map the input PWM source for half-bridges 5-8.

Figure 8-13. PWM_CTRL2 Register

7	6	5	4	3	2	1	0
HB5_PWM		HB6_PWM		HB7_PWM		HB8_PWM	
R/W-10b		R/W-10b		R/W-11b		R/W-11b	

Table 8-21. PWM_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HB5_PWM	R/W	10b	Configure PWM input source for half-bridge 5. 00b = IN1 01b = IN2 10b = IN3 11b = IN4
5-4	HB6_PWM	R/W	10b	Configure PWM input source for half-bridge 6. 00b = IN1 01b = IN2 10b = IN3 11b = IN4
3-2	HB7_PWM	R/W	11b	Configure PWM input source for half-bridge 7. 00b = IN1 01b = IN2 10b = IN3 11b = IN4
1-0	HB8_PWM	R/W	11b	Configure PWM input source for half-bridge 8. 00b = IN1 01b = IN2 10b = IN3 11b = IN4

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8.3.2.7 PWM_CTRL3 Register (Address = Dh) [Reset = 0h]

PWM_CTRL3 is shown in Figure 8-14 and described in Table 8-22.

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Control register to set the PWM drive MOSFET (high or low) for half-bridges 1-8.

Figure 8-14. PWM_CTRL3 Register

7	6	5	4	3	2	1	0
HB1_HL	HB2_HL	HB3_HL	HB4_HL	HB5_HL	HB6_HL	HB7_HL	HB8_HL
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-22. PWM_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HB1_HL	R/W	0b	Set half-bridge 1 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
6	HB2_HL	R/W	0b	Set half-bridge 2 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
5	HB3_HL	R/W	0b	Set half-bridge 3 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
4	HB4_HL	R/W	0b	Set half-bridge 4 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
3	HB5_HL	R/W	0b	Set half-bridge 5 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
2	HB6_HL	R/W	0b	Set half-bridge 6 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
1	HB7_HL	R/W	0b	Set half-bridge 7 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
0	HB8_HL	R/W	0b	Set half-bridge 8 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.

8.3.2.8 PWM_CTRL4 Register (Address = Eh) [Reset = 0h]

PWM_CTRL4 is shown in Figure 8-15 and described in Table 8-23.

Return to the Summary Table.

Control register to set the PWM freewheeling mode for half-bridges 1-8.

Figure 8-15. PWM_CTRL4 Register

7	6	5	4	3	2	1	0
HB1_FW	HB2_FW	HB3_FW	HB4_FW	HB5_FW	HB6_FW	HB7_FW	HB8_FW
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-23. PWM_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HB1_FW	R/W	0b	Configure freewheeling setting for half-bridge 1. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.

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Table 8-23. PWM_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	HB2_FW	R/W	0b	Configure freewheeling setting for half-bridge 2. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
5	HB3_FW	R/W	0b	Configure freewheeling setting for half-bridge 3. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
4	HB4_FW	R/W	0b	Configure freewheeling setting for half-bridge 4. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
3	HB5_FW	R/W	0b	Configure freewheeling setting for half-bridge 5. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
2	HB6_FW	R/W	0b	Configure freewheeling setting for half-bridge 6. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
1	HB7_FW	R/W	0b	Configure freewheeling setting for half-bridge 7. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
0	HB8_FW	R/W	0b	Configure freewheeling setting for half-bridge 8. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.

8.3.2.9 IDRV_CTRL1 Register (Address = Fh) [Reset = FFh]

IDRV_CTRL1 is shown in Figure 8-16 and described in Table 8-24.

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Control register to configure the source and sink current for the half-bridge 1 high-side and low-side gate drivers.

Figure 8-16. IDRV_CTRL1 Register

7	6	5	4	3	2	1	0
IDRVP_1				IDRVN_1			
R/W-1111b				R/W-1111b			

Table 8-24. IDRV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_1	R/W	1111b	Half-bridge 1 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO1). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

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Table 8-24. IDRV_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_1	R/W	1111b	Half-bridge 1 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO1). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.3.2.10 IDRV_CTRL2 Register (Address = 10h) [Reset = FFh]

IDRV_CTRL2 is shown in Figure 8-17 and described in Table 8-25.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 2 high-side and low-side gate drivers.

Figure 8-17. IDRV_CTRL2 Register

7	6	5	4	3	2	1	0
IDRVP_2				IDRVN_2			
R/W-1111b				R/W-1111b			

Table 8-25. IDRV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_2	R/W	1111b	Half-bridge 2 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO2). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

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Table 8-25. IDRV_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_2	R/W	1111b	Half-bridge 2 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO2). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.3.2.11 IDRV_CTRL3 Register (Address = 11h) [Reset = FFh]

IDRV_CTRL3 is shown in Figure 8-18 and described in Table 8-26.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 3 high-side and low-side gate drivers.

Figure 8-18. IDRV_CTRL3 Register

7	6	5	4	3	2	1	0
IDRVP_3				IDRVN_3			
R/W-1111b				R/W-1111b			

Table 8-26. IDRV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_3	R/W	1111b	Half-bridge 3 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO3). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

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Table 8-26. IDRV_CTRL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_3	R/W	1111b	Half-bridge 3 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO3). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.3.2.12 IDRV_CTRL4 Register (Address = 12h) [Reset = FFh]

IDRV_CTRL4 is shown in Figure 8-19 and described in Table 8-27.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 4 high-side and low-side gate drivers.

Figure 8-19. IDRV_CTRL4 Register

7	6	5	4	3	2	1	0
IDRVP_4				IDRVN_4			
R/W-1111b				R/W-1111b			

Table 8-27. IDRV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_4	R/W	1111b	Half-bridge 4 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO4). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

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Table 8-27. IDRV_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_4	R/W	1111b	Half-bridge 4 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO4). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.3.2.13 IDRV_CTRL5 Register (Address = 13h) [Reset = FFh]

IDRV_CTRL5 is shown in Figure 8-20 and described in Table 8-28.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 5 high-side and low-side gate drivers.

Figure 8-20. IDRV_CTRL5 Register

7	6	5	4	3	2	1	0
IDRVP_5				IDRVN_5			
R/W-1111b				R/W-1111b			

Table 8-28. IDRV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_5	R/W	1111b	Half-bridge 5 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO5). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

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Table 8-28. IDRV_CTRL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_5	R/W	1111b	Half-bridge 5 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO5). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.3.2.14 IDRV_CTRL6 Register (Address = 14h) [Reset = FFh]

IDRV_CTRL6 is shown in Figure 8-21 and described in Table 8-29.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 6 high-side and low-side gate drivers.

Figure 8-21. IDRV_CTRL6 Register

7	6	5	4	3	2	1	0
IDRVP_6				IDRVN_6			
R/W-1111b				R/W-1111b			

Table 8-29. IDRV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_6	R/W	1111b	Half-bridge 6 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO6). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

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Table 8-29. IDRV_CTRL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_6	R/W	1111b	Half-bridge 6 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO6). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.3.2.15 IDRV_CTRL7 Register (Address = 15h) [Reset = FFh]

IDRV_CTRL7 is shown in Figure 8-22 and described in Table 8-30.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 7 high-side and low-side gate drivers.

Figure 8-22. IDRV_CTRL7 Register

7	6	5	4	3	2	1	0
IDRVP_7				IDRVN_7			
R/W-1111b				R/W-1111b			

Table 8-30. IDRV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_7	R/W	1111b	Half-bridge 7 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO7). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

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Table 8-30. IDRV_CTRL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_7	R/W	1111b	Half-bridge 7 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO7). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.3.2.16 IDRV_CTRL8 Register (Address = 16h) [Reset = FFh]

IDRV_CTRL8 is shown in Figure 8-23 and described in Table 8-31.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 8 high-side and low-side gate drivers.

Figure 8-23. IDRV_CTRL8 Register

7	6	5	4	3	2	1	0
IDRVP_8				IDRVN_8			
R/W-1111b				R/W-1111b			

Table 8-31. IDRV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_8	R/W	1111b	Half-bridge 8 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO8). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

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Table 8-31. IDRV_CTRL8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	IDRVN_8	R/W	1111b	Half-bridge 8 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO8). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.3.2.17 IDRV_CTRL9 Register (Address = 17h) [Reset = 0h]

IDRV_CTRL9 is shown in Figure 8-24 and described in Table 8-32.

Return to the Summary Table.

Control register to enable ultra-low source and sink current settings for half-bridges 1-8.

Figure 8-24. IDRV_CTRL9 Register

7	6	5	4	3	2	1	0
IDRV_LO1	IDRV_LO2	IDRV_LO3	IDRV_LO4	IDRV_LO5	IDRV_LO6	IDRV_LO7	IDRV_LO8
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-32. IDRV_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IDRV_LO1	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 1. 0b = IDRVP_1 and IDRVN_1 utilize standard values. 1b = IDRVP_1 and IDRVN_1 utilize low current values.
6	IDRV_LO2	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 2. 0b = IDRVP_2 and IDRVN_2 utilize standard values. 1b = IDRVP_2 and IDRVN_2 utilize low current values.
5	IDRV_LO3	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 3. 0b = IDRVP_3 and IDRVN_3 utilize standard values. 1b = IDRVP_3 and IDRVN_3 utilize low current values.
4	IDRV_LO4	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 4. 0b = IDRVP_4 and IDRVN_4 utilize standard values. 1b = IDRVP_4 and IDRVN_4 utilize low current values.
3	IDRV_LO5	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 5. 0b = IDRVP_5 and IDRVN_5 utilize standard values. 1b = IDRVP_5 and IDRVN_5 utilize low current values.
2	IDRV_LO6	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 6. 0b = IDRVP_6 and IDRVN_6 utilize standard values. 1b = IDRVP_6 and IDRVN_6 utilize low current values.
1	IDRV_LO7	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 7. 0b = IDRVP_7 and IDRVN_7 utilize standard values. 1b = IDRVP_7 and IDRVN_7 utilize low current values.

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Table 8-32. IDRV_CTRL9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IDRV_LO8	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 8. 0b = IDRVP_8 and IDRVN_8 utilize standard values. 1b = IDRVP_8 and IDRVN_8 utilize low current values.

8.3.2.18 DRV_CTRL1 Register (Address = 18h) [Reset = 0h]

DRV_CTRL1 is shown in Figure 8-25 and described in Table 8-33.

Return to the Summary Table.

Control register to set the VGS and VDS monitor operating modes and configurations.

Figure 8-25. DRV_CTRL1 Register

7	6	5	4	3	2	1	0
VGS_MODE		VGS_IND	VGS_LVL	VGS_HS_DIS	VDS_MODE		VDS_IND
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b

Table 8-33. DRV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VGS_MODE	R/W	00b	VGS gate fault monitor mode for half-bridges 1-8. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5	VGS_IND	R/W	0b	VGS fault independent shutdown mode configuration. 0b = Disabled. VGS fault will shut down all half-bridge drivers. 1b = Enabled. VGS gate fault will only shutdown the associated half-bridge driver.
4	VGS_LVL	R/W	0b	VGS threshold comparator level for dead-time handshake and VGS fault monitor for half-bridge drivers. 0b = 1.4 V 1b = 1 V
3	VGS_HS_DIS	R/W	0b	VGS dead-time handshake monitor disable. 0b = 0x0 1b = Disabled. Half-bridge transition is based only on TDRIVE and programmable digital dead-time delays.
2-1	VDS_MODE	R/W	00b	VDS overcurrent monitor mode for half-bridges 1-8. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
0	VDS_IND	R/W	0b	VDS fault independent shutdown mode configuration. 0b = Disabled. VDS fault will shut down all half-bridge drivers. 1b = Enabled. VDS gate fault will only shutdown the associated half-bridge driver.

8.3.2.19 DRV_CTRL2 Register (Address = 19h) [Reset = 12h]

DRV_CTRL2 is shown in Figure 8-26 and described in Table 8-34.

Return to the Summary Table.

Control register to set tDRV, the VGS drive and VDS monitor blanking time for half-bridges 1-4.

Figure 8-26. DRV_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED		VGS_TDRV_12			VGS_TDRV_34		

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Figure 8-26. DRV_CTRL2 Register (continued)

R-00b	R/W-010b	R/W-010b

Table 8-34. DRV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-3	VGS_TDRV_12	R/W	010b	VGS drive and VDS monitor blanking time for half-bridge 1 and 2. 000b = 2 µs 001b = 4 µs 010b = 8 µs 011b = 12 µs 100b = 16 µs 101b = 24 µs 110b = 32 µs 111b = 96 µs
2-0	VGS_TDRV_34	R/W	010b	VGS drive and VDS monitor blanking time for half-bridge 3 and 4. 000b = 2 µs 001b = 4 µs 010b = 8 µs 011b = 12 µs 100b = 16 µs 101b = 24 µs 110b = 32 µs 111b = 96 µs

8.3.2.20 DRV_CTRL3 Register (Address = 1Ah) [Reset = 12h]

DRV_CTRL3 is shown in Figure 8-27 and described in Table 8-35.

Return to the Summary Table.

Control register to set tDRV, the VGS drive and VDS monitor blanking time for half-bridges 5-8.

Figure 8-27. DRV_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		VGS_TDRV_56			VGS_TDRV_78		
R-00b		R/W-010b			R/W-010b		

Table 8-35. DRV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-3	VGS_TDRV_56	R/W	010b	VGS drive and VDS monitor blanking time for half-bridge 5 and 6. 000b = 2 µs 001b = 4 µs 010b = 8 µs 011b = 12 µs 100b = 16 µs 101b = 24 µs 110b = 32 µs 111b = 96 µs
2-0	VGS_TDRV_78	R/W	010b	VGS drive and VDS monitor blanking time for half-bridge 7 and 8. 000b = 2 µs 001b = 4 µs 010b = 8 µs 011b = 12 µs 100b = 16 µs 101b = 24 µs 110b = 32 µs 111b = 96 µs

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8.3.2.21 DRV_CTRL4 Register (Address = 1Bh) [Reset = 0h]

DRV_CTRL4 is shown in Figure 8-28 and described in Table 8-36.

Return to the Summary Table.

Control register to set VGS tDEAD_D, additional digital dead-time insertion for half-bridges 1-8.

Figure 8-28. DRV_CTRL4 Register

7	6	5	4	3	2	1	0
VGS_TDEAD_12		VGS_TDEAD_34		VGS_TDEAD_56		VGS_TDEAD_78	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-36. DRV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VGS_TDEAD_12	R/W	00b	Insertable digital dead-time for half-bridge 1 and 2. 00b = 0 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
5-4	VGS_TDEAD_34	R/W	00b	Insertable digital dead-time for half-bridge 3 and 4. 00b = 0 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
3-2	VGS_TDEAD_56	R/W	00b	Insertable digital dead-time for half-bridge 5 and 6. 00b = 0 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
1-0	VGS_TDEAD_78	R/W	00b	Insertable digital dead-time for half-bridge 7 and 8. 00b = 0 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs

8.3.2.22 DRV_CTRL5 Register (Address = 1Ch) [Reset = AAh]

DRV_CTRL5 is shown in Figure 8-29 and described in Table 8-37.

Return to the Summary Table.

Control register to set VDS tDS_DG, overcurrent monitor deglitch time for half-bridges 1-8.

Figure 8-29. DRV_CTRL5 Register

7	6	5	4	3	2	1	0
VDS_DG_12		VDS_DG_34		VDS_DG_56		VDS_DG_78	
R/W-10b		R/W-10b		R/W-10b		R/W-10b	

Table 8-37. DRV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VDS_DG_12	R/W	10b	VDS overcurrent monitor deglitch time for half-bridge 1 and 2. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs

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Table 8-37. DRV_CTRL5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VDS_DG_34	R/W	10b	VDS overcurrent monitor deglitch time for half-bridge 3 and 4. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
3-2	VDS_DG_56	R/W	10b	VDS overcurrent monitor deglitch time for half-bridge 5 and 6. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
1-0	VDS_DG_78	R/W	10b	VDS overcurrent monitor deglitch time for half-bridge 7 and 8. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs

8.3.2.23 DRV_CTRL6 Register (Address = 1Dh) [Reset = 0h]

DRV_CTRL6 is shown in Figure 8-30 and described in Table 8-38.

Return to the Summary Table.

Control register to set the gate pulldown current (IDRVN) in response to VDS overcurrent fault for half-bridges 1-8.

Figure 8-30. DRV_CTRL6 Register

7	6	5	4	3	2	1	0
VDS_IDRVN_12		VDS_IDRVN_34		VDS_IDRVN_56		VDS_IDRVN_78	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-38. DRV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VDS_IDRVN_12	R/W	00b	IDRVN gate pulldown current after VDS_OCP fault for half-bridge 1 and 2. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA
5-4	VDS_IDRVN_34	R/W	00b	IDRVN gate pulldown current after VDS_OCP fault for half-bridge 3 and 4. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA
3-2	VDS_IDRVN_56	R/W	00b	IDRVN gate pulldown current after VDS_OCP fault for half-bridge 5 and 6. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA
1-0	VDS_IDRVN_78	R/W	00b	IDRVN gate pulldown current after VDS_OCP fault for half-bridge 7 and 8. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA

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8.3.2.24 VDS_CTRL1 Register (Address = 1Fh) [Reset = DDh]

VDS_CTRL1 is shown in Figure 8-31 and described in Table 8-39.

Return to the Summary Table.

Control register to set the VDS overcurrent monitor voltage threshold for half-bridges 1 and 2.

Figure 8-31. VDS_CTRL1 Register

7	6	5	4	3	2	1	0
VDS_LVL_1				VDS_LVL_2			
R/W-1101b				R/W-1101b			

Table 8-39. VDS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	VDS_LVL_1	R/W	1101b	Half-bridge 1 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V
3-0	VDS_LVL_2	R/W	1101b	Half-bridge 2 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

8.3.2.25 VDS_CTRL2 Register (Address = 20h) [Reset = DDh]

VDS_CTRL2 is shown in Figure 8-32 and described in Table 8-40.

Return to the Summary Table.

Control register to set the VDS overcurrent monitor voltage threshold for half-bridges 3 and 4.

Figure 8-32. VDS_CTRL2 Register

7	6	5	4	3	2	1	0
VDS_LVL_3				VDS_LVL_4			
R/W-1101b				R/W-1101b			

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Figure 8-32. VDS_CTRL2 Register (continued)

Table 8-40. VDS_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	VDS_LVL_3	R/W	1101b	Half-bridge 3 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V
3-0	VDS_LVL_4	R/W	1101b	Half-bridge 4 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

8.3.2.26 VDS_CTRL3 Register (Address = 21h) [Reset = DDh]

VDS_CTRL3 is shown in Figure 8-33 and described in Table 8-41.

Return to the Summary Table.

Control register to set the VDS overcurrent monitor voltage threshold for half-bridges 5 and 6.

Figure 8-33. VDS_CTRL3 Register

7	6	5	4	3	2	1	0
VDS_LVL_5				VDS_LVL_6			
R/W-1101b				R/W-1101b			

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Table 8-41. VDS_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	VDS_LVL_5	R/W	1101b	Half-bridge 5 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V
3-0	VDS_LVL_6	R/W	1101b	Half-bridge 6 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

8.3.2.27 VDS_CTRL4 Register (Address = 22h) [Reset = DDh]

VDS_CTRL4 is shown in Figure 8-34 and described in Table 8-42.

Return to the Summary Table.

Control register to set the VDS overcurrent monitor voltage threshold for half-bridges 7 and 8.

Figure 8-34. VDS_CTRL4 Register

7	6	5	4	3	2	1	0
VDS_LVL_7				VDS_LVL_8			
R/W-1101b				R/W-1101b			

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Table 8-42. VDS_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	VDS_LVL_7	R/W	1101b	Half-bridge 7 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V
3-0	VDS_LVL_8	R/W	1101b	Half-bridge 8 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

8.3.2.28 OLSC_CTRL1 Register (Address = 23h) [Reset = 0h]

OLSC_CTRL1 is shown in Figure 8-35 and described in Table 8-43.

Return to the Summary Table.

Control register to enable and disable the offline diagnostic current sources for half-bridges 1-4.

Figure 8-35. OLSC_CTRL1 Register

7	6	5	4	3	2	1	0
PU_SH1	PD_SH1	PU_SH2	PD_SH2	PU_SH3	PD_SH3	PU_SH4	PD_SH4
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-43. OLSC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PU_SH1	R/W	0b	Half-bridge 1 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
6	PD_SH1	R/W	0b	Half-bridge 1 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.

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Table 8-43. OLSC_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PU_SH2	R/W	0b	Half-bridge 2 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
4	PD_SH2	R/W	0b	Half-bridge 2 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
3	PU_SH3	R/W	0b	Half-bridge 3 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
2	PD_SH3	R/W	0b	Half-bridge 3 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
1	PU_SH4	R/W	0b	Half-bridge 4 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
0	PD_SH4	R/W	0b	Half-bridge 4 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.

8.3.2.29 OLSC_CTRL2 Register (Address = 24h) [Reset = 0h]

OLSC_CTRL2 is shown in Figure 8-36 and described in Table 8-44.

Return to the Summary Table.

Control register to enable and disable the offline diagnostic current sources for half-bridges 5-8.

Figure 8-36. OLSC_CTRL2 Register

7	6	5	4	3	2	1	0
PU_SH5	PD_SH5	PU_SH6	PD_SH6	PU_SH7	PD_SH7	PU_SH8	PD_SH8
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-44. OLSC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PU_SH5	R/W	0b	Half-bridge 5 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
6	PD_SH5	R/W	0b	Half-bridge 5 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
5	PU_SH6	R/W	0b	Half-bridge 6 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
4	PD_SH6	R/W	0b	Half-bridge 6 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.

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Table 8-44. OLSC_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PU_SH7	R/W	0b	Half-bridge 7 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
2	PD_SH7	R/W	0b	Half-bridge 7 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
1	PU_SH8	R/W	0b	Half-bridge 8 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
0	PD_SH8	R/W	0b	Half-bridge 8 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.

8.3.2.30 UVOV_CTRL Register (Address = 25h) [Reset = 14h]

UVOV_CTRL is shown in Figure 8-37 and described in Table 8-45.

Return to the Summary Table.

Control register to set the undervoltage and overvoltage monitor configurations.

Figure 8-37. UVOV_CTRL Register

7	6	5	4	3	2	1	0
PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_DG		PVDD_OV_LVL	VCP_UV_MODE	VCP_UV_LVL
R/W-0b	R/W-00b		R/W-10b		R/W-1b	R/W-0b	R/W-0b

Table 8-45. UVOV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_UV_MODE	R/W	0b	PVDD supply undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
6-5	PVDD_OV_MODE	R/W	00b	PVDD supply overvoltage monitor mode. 00b = Latched fault. 01b = Automatic recovery. 10b = Warning report only. 11b = Disabled.
4-3	PVDD_OV_DG	R/W	10b	PVDD supply overvoltage monitor deglitch time. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
2	PVDD_OV_LVL	R/W	1b	PVDD supply overvoltage monitor threshold. 0b = 21.5 V 1b = 28.5 V
1	VCP_UV_MODE	R/W	0b	VCP charge pump undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
0	VCP_UV_LVL	R/W	0b	VCP charge pump undervoltage monitor threshold. 0b = 4.75 V 1b = 6.25 V

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8.3.2.31 CSA_CTRL1 Register (Address = 26h) [Reset = 9h]

CSA_CTRL1 is shown in Figure 8-38 and described in Table 8-46.

Return to the Summary Table.

Control register for gain and reference voltage for shunt amplifier 1 and 2.

Figure 8-38. CSA_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED		CSA_DIV_1	CSA_GAIN_1		CSA_DIV_2	CSA_GAIN_2	
R-00b		R/W-0b	R/W-01b		R/W-0b	R/W-01b	

Table 8-46. CSA_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5	CSA_DIV_1	R/W	0b	Current shunt amplifier 1 reference voltage divider. 0b = AREF / 2 1b = AREF / 8
4-3	CSA_GAIN_1	R/W	01b	Current shunt amplifier 1 gain setting. 00b = 10 V/V 01b = 20 V/V 10b = 40 V/V 11b = 80 V/V
2	CSA_DIV_2	R/W	0b	Current shunt amplifier 2 reference voltage divider. 0b = AREF / 2 1b = AREF / 8
1-0	CSA_GAIN_2	R/W	01b	Current shunt amplifier 2 gain setting. 00b = 10 V/V 01b = 20 V/V 10b = 40 V/V 11b = 80 V/V

8.3.2.32 CSA_CTRL2 Register (Address = 27h) [Reset = 0h]

CSA_CTRL2 is shown in Figure 8-39 and described in Table 8-47.

Return to the Summary Table.

Control register for shunt amplifier 1 blanking configuration.

Figure 8-39. CSA_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED		CSA_BLK_SEL_1			CSA_BLK_LVL_1		
R-00b		R/W-000b			R/W-000b		

Table 8-47. CSA_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-3	CSA_BLK_SEL_1	R/W	000b	Current shunt amplifier 1 blanking trigger source. 000b = Half-bridge 1 001b = Half-bridge 2 010b = Half-bridge 3 011b = Half-bridge 4 100b = Half-bridge 5 101b = Half-bridge 6 110b = Half-bridge 7 111b = Half-bridge 8

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Table 8-47. CSA_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	CSA_BLK_LVL_1	R/W	000b	Current shunt amplifier 1 blanking time. % of tDRV. 000b = 0 %, Disabled 001b = 25 % 010b = 37.5 % 011b = 50 % 100b = 62.5 % 101b = 75 % 110b = 87.5 % 111b = 100 %

8.3.2.33 CSA_CTRL3 Register (Address = 28h) [Reset = 20h]

CSA_CTRL3 is shown in Figure 8-40 and described in Table 8-48.

Return to the Summary Table.

Control register for shunt amplifier 2 blanking configuration.

Figure 8-40. CSA_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		CSA_BLK_SEL_2			CSA_BLK_LVL_2		
R-00b		R/W-100b			R/W-000b		

Table 8-48. CSA_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-3	CSA_BLK_SEL_2	R/W	100b	Current shunt amplifier 2 blanking trigger source. 000b = Half-bridge 1 001b = Half-bridge 2 010b = Half-bridge 3 011b = Half-bridge 4 100b = Half-bridge 5 101b = Half-bridge 6 110b = Half-bridge 7 111b = Half-bridge 8
2-0	CSA_BLK_LVL_2	R/W	000b	Current shunt amplifier 2 blanking time. % of tDRV. 000b = 0 %, Disabled 001b = 25 % 010b = 37.5 % 011b = 50 % 100b = 62.5 % 101b = 75 % 110b = 87.5 % 111b = 100 %

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8.3.3 DRV8718-Q1_CONTROL_ADV Registers

Table 8-49 lists the DRV8718-Q1_CONTROL_ADV registers. All register offset addresses not listed in Table 8-49 should be considered as reserved locations and the register contents should not be modified.

Table 8-49. DRV8718-Q1_CONTROL_ADV Registers

Address	Acronym	Register Name	Section
2Ah	AGD_CTRL1	Adaptive gate drive general control functions	Go
2Bh	PDR_CTRL1	Half-bridge 1 and 2 PDR delay and max current settings	Go
2Ch	PDR_CTRL2	Half-bridge 3 and 4 PDR delay and max current settings	Go
2Dh	PDR_CTRL3	Half-bridge 5 and 6 PDR delay and max current settings	Go
2Eh	PDR_CTRL4	Half-bridge 7 and 8 PDR delay and max current settings	Go
2Fh	PDR_CTRL5	Half-bridge 1 and 2 PDR charge and discharge initial settings.	Go
30h	PDR_CTRL6	Half-bridge 3 and 4 PDR charge and discharge initial settings.	Go
31h	PDR_CTRL7	Half-bridge 5 and 6 PDR charge and discharge initial settings.	Go
32h	PDR_CTRL8	Half-bridge 7 and 8 PDR charge and discharge initial settings.	Go
33h	PDR_CTRL9	Half-bridge 1-4 PDR loop controller gain	Go
34h	PDR_CTRL10	Half-bridge 5-8 PDR loop controller gain	Go
35h	STC_CTRL1	Half-bridge 1 and 2 STC rise/fall time and controller gain	Go
36h	STC_CTRL2	Half-bridge 3 and 4 STC rise/fall time and controller gain	Go
37h	STC_CTRL3	Half-bridge 5 and 6 STC rise/fall time and controller gain	Go
38h	STC_CTRL4	Half-bridge 7 and 8 STC rise/fall time and controller gain	Go
39h	DCC_CTRL1	Half-bridge 1-8 DCC enable and manual control	Go
3Ah	PST_CTRL1	Half-bridge 1-8 freewheel and post charge delay control	Go
3Bh	PST_CTRL2	Half-bridge 1-8 post charge controller gain	Go

Complex bit access types are encoded to fit into small table cells. Table 8-50 shows the codes that are used for access types in this section.

Table 8-50. DRV8718-Q1_CONTROL_ADV Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
- *n*		Value after reset or the default value

8.3.3.1 AGD_CTRL1 Register (Address = 2Ah) [Reset = 40h]

AGD_CTRL1 is shown in Figure 8-41 and described in Table 8-51.

Return to the Summary Table.

Control register for adaptive gate drive voltage thresholds, pull down setting, and active half-bridge configuration.

Figure 8-41. AGD_CTRL1 Register

7	6	5	4	3	2	1	0
AGD_THR		AGD_ISTRONG		SET_AGD_12	SET_AGD_34	SET_AGD_56	SET_AGD_78

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Figure 8-41. AGD_CTRL1 Register (continued)

R/W-01b	R/W-00b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-51. AGD_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	AGD_THR	R/W	01b	Adaptive gate driver VSH threshold configuration. 00b = 1V, VDRAIN - 0.5V 01b = 1V, VDRAIN - 1V 10b = 2V, VDRAIN - 1.5V 11b = 2V, VDRAIN - 2V
5-4	AGD_ISTRONG	R/W	00b	Adaptive gate driver ISTRONG configuration. 00b = ISTRONG pulldown decoded from initial IDRVP_x register setting. 01b = 62 mA 10b = 124 mA 11b = RSVD
3	SET_AGD_12	R/W	0b	Set active half-bridge for adaptive gate drive control loops. 0b = Half-bridge 1 1b = Half-bridge 2
2	SET_AGD_34	R/W	0b	Set active half-bridge for adaptive gate drive control loops. 0b = Half-bridge 3 1b = Half-bridge 4
1	SET_AGD_56	R/W	0b	Set active half-bridge for adaptive gate drive control loops. 0b = Half-bridge 5 1b = Half-bridge 6
0	SET_AGD_78	R/W	0b	Set active half-bridge for adaptive gate drive control loops. 0b = Half-bridge 7 1b = Half-bridge 8

8.3.3.2 PDR_CTRL1 Register (Address = 2Bh) [Reset = Ah]

PDR_CTRL1 is shown in Figure 8-42 and described in Table 8-52.

Return to the Summary Table.

Control register for tON_OFF propagation delay and pre-charge/discharge max current for half-bridges 1 and 2.

Figure 8-42. PDR_CTRL1 Register

7	6	5	4	3	2	1	0
PRE_MAX_12		T_DON_DOFF_12					
R/W-00b		R/W-001010b					

Table 8-52. PDR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRE_MAX_12	R/W	00b	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 1 and 2. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA
5-0	T_DON_DOFF_12	R/W	001010b	On and off time delay for half-bridge 1 and 2. 140 ns x T_DON_DOFF_12 [3:0] Default time: 001010b (1.4 us)

8.3.3.3 PDR_CTRL2 Register (Address = 2Ch) [Reset = Ah]

PDR_CTRL2 is shown in Figure 8-43 and described in Table 8-53.

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Return to the Summary Table.

Control register for tON_OFF propagation delay and pre-charge/discharge max current for half-bridges 3 and 4.

Figure 8-43. PDR_CTRL2 Register

7	6	5	4	3	2	1	0
PRE_MAX_34		T_DON_DOFF_34					
R/W-00b		R/W-001010b					

Table 8-53. PDR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRE_MAX_34	R/W	00b	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 3 and 4. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA
5-0	T_DON_DOFF_34	R/W	001010b	On and off time delay for half-bridge 3 and 4. 140 ns x T_DON_DOFF_34 [3:0] Default time: 001010b (1.4 us)

8.3.3.4 PDR_CTRL3 Register (Address = 2Dh) [Reset = Ah]

PDR_CTRL3 is shown in Figure 8-44 and described in Table 8-54.

Return to the Summary Table.

Control register for tON_OFF propagation delay and pre-charge/discharge max current for half-bridges 5 and 6.

Figure 8-44. PDR_CTRL3 Register

7	6	5	4	3	2	1	0
PRE_MAX_56		T_DON_DOFF_56					
R/W-00b		R/W-001010b					

Table 8-54. PDR_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRE_MAX_56	R/W	00b	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 5 and 6. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA
5-0	T_DON_DOFF_56	R/W	001010b	On and off time delay for half-bridge 5 and 6. 140 ns x T_DON_DOFF_56 [3:0] Default time: 001010b (1.4 us)

8.3.3.5 PDR_CTRL4 Register (Address = 2Eh) [Reset = Ah]

PDR_CTRL4 is shown in Figure 8-45 and described in Table 8-55.

Return to the Summary Table.

Control register for tON_OFF propagation delay and pre-charge/discharge max current for half-bridges 7 and 8.

Figure 8-45. PDR_CTRL4 Register

7	6	5	4	3	2	1	0
PRE_MAX_78		T_DON_DOFF_78					
R/W-00b		R/W-001010b					

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Table 8-55. PDR_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRE_MAX_78	R/W	00b	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 7 and 8. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA
5-0	T_DON_DOFF_78	R/W	001010b	On and off time delay for half-bridge 7 and 8. 140 ns x T_DON_DOFF_78 [3:0] Default time: 001010b (1.4 us)

8.3.3.6 PDR_CTRL5 Register (Address = 2Fh) [Reset = F6h]

PDR_CTRL5 is shown in Figure 8-46 and described in Table 8-56.

Return to the Summary Table.

Control register for charge and pre-charge initial settings for half-bridges 1 and 2.

Figure 8-46. PDR_CTRL5 Register

7	6	5	4	3	2	1	0
T_PRE_CHR_12		T_PRE_DCHR_12		PRE_CHR_INIT_12		PRE_DCHR_INIT_12	
R/W-11b		R/W-11b		R/W-01b		R/W-10b	

Table 8-56. PDR_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	T_PRE_CHR_12	R/W	11b	PDR control loop pre-charge time for half-bridge 1 and 2. Set as ratio of T_DON_DOFF_12 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR_12	R/W	11b	PDR control loop pre-discharge time for half-bridge 1 and 2. Set as ratio of T_DON_DOFF_12 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT_12	R/W	01b	PDR control loop initial pre-charge current setting for half-bridge 1 and 2. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA
1-0	PRE_DCHR_INIT_12	R/W	10b	PDR control loop initial pre-discharge current setting for half-bridge 1 and 2.. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.3.3.7 PDR_CTRL6 Register (Address = 30h) [Reset = F6h]

PDR_CTRL6 is shown in Figure 8-47 and described in Table 8-57.

Return to the Summary Table.

Control register for charge and pre-charge initial settings for half-bridges 3 and 4.

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Figure 8-47. PDR_CTRL6 Register

7	6	5	4	3	2	1	0
T_PRE_CHR_34		T_PRE_DCHR_34		PRE_CHR_INIT_34		PRE_DCHR_INIT_34	
R/W-11b		R/W-11b		R/W-01b		R/W-10b	

Table 8-57. PDR_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	T_PRE_CHR_34	R/W	11b	PDR control loop pre-charge time for half-bridge 3 and 4. Set as ratio of T_DON_DOFF_34 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR_34	R/W	11b	PDR control loop pre-discharge time for half-bridge 3 and 4. Set as ratio of T_DON_DOFF_34 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT_34	R/W	01b	PDR control loop initial pre-charge current setting for half-bridge 3 and 4. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA
1-0	PRE_DCHR_INIT_34	R/W	10b	PDR control loop initial pre-discharge current setting for half-bridge 3 and 4. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.3.3.8 PDR_CTRL7 Register (Address = 31h) [Reset = F6h]

PDR_CTRL7 is shown in Figure 8-48 and described in Table 8-58.

Return to the Summary Table.

Control register for charge and pre-charge initial settings for half-bridges 5 and 6.

Figure 8-48. PDR_CTRL7 Register

7	6	5	4	3	2	1	0
T_PRE_CHR_56		T_PRE_DCHR_56		PRE_CHR_INIT_56		PRE_DCHR_INIT_56	
R/W-11b		R/W-11b		R/W-01b		R/W-10b	

Table 8-58. PDR_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	T_PRE_CHR_56	R/W	11b	PDR control loop pre-charge time for half-bridge 5 and 6. Set as ratio of T_DON_DOFF_56 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR_56	R/W	11b	PDR control loop pre-discharge time for half-bridge 5 and 6. Set as ratio of T_DON_DOFF_56 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2

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Table 8-58. PDR_CTRL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PRE_CHR_INIT_56	R/W	01b	PDR control loop initial pre-charge current setting for half-bridge 5 and 6. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA
1-0	PRE_DCHR_INIT_56	R/W	10b	PDR control loop initial pre-discharge current setting for half-bridge 5 and 6. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.3.3.9 PDR_CTRL8 Register (Address = 32h) [Reset = F6h]

PDR_CTRL8 is shown in Figure 8-49 and described in Table 8-59.

Return to the Summary Table.

Control register for charge and pre-charge initial settings for half-bridges 7 and 8.

Figure 8-49. PDR_CTRL8 Register

7	6	5	4	3	2	1	0
T_PRE_CHR_78		T_PRE_DCHR_78		PRE_CHR_INIT_78		PRE_DCHR_INIT_78	
R/W-11b		R/W-11b		R/W-01b		R/W-10b	

Table 8-59. PDR_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	T_PRE_CHR_78	R/W	11b	PDR control loop pre-charge time for half-bridge 7 and 8. Set as ratio of T_DON_DOFF_78 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR_78	R/W	11b	PDR control loop pre-discharge time for half-bridge 7 and 8. Set as ratio of T_DON_DOFF_78 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT_78	R/W	01b	PDR control loop initial pre-charge current setting for half-bridge 7 and 8. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA
1-0	PRE_DCHR_INIT_78	R/W	10b	PDR control loop initial pre-discharge current setting for half-bridge 7 and 8. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.3.3.10 PDR_CTRL9 Register (Address = 33h) [Reset = 11h]

PDR_CTRL9 is shown in Figure 8-50 and described in Table 8-60.

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Return to the Summary Table.

Control register to configure PDR Kp loop controller gain setting for half-bridges 1-4.

Figure 8-50. PDR_CTRL9 Register

7	6	5	4	3	2	1	0
EN_PDR_12	PDR_ERR_12	KP_PDR_12		EN_PDR_34	PDR_ERR_34	KP_PDR_34	
R/W-0b	R/W-0b	R/W-01b		R/W-0b	R/W-0b	R/W-01b	

Table 8-60. PDR_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_PDR_12	R/W	0b	Enable PDR loop control for half-bridge 1 and 2.
6	PDR_ERR_12	R/W	0b	PDR loop error limit for half-bridge 1 and 2. 0b = 1-bit error 1b = Actual error
5-4	KP_PDR_12	R/W	01b	PDR proportional controller gain setting for half-bridge 1 and 2. 00b = 1 01b = 2 10b = 3 11b = 4
3	EN_PDR_34	R/W	0b	Enable PDR loop control for half-bridge 3 and 4.
2	PDR_ERR_34	R/W	0b	PDR loop error limit for half-bridge 3 and 4. 0b = 1-bit error 1b = Actual error
1-0	KP_PDR_34	R/W	01b	PDR proportional controller gain setting for half-bridge 3 and 4. 00b = 1 01b = 2 10b = 3 11b = 4

8.3.3.11 PDR_CTRL10 Register (Address = 34h) [Reset = 11h]

PDR_CTRL10 is shown in Figure 8-51 and described in Table 8-61.

Return to the Summary Table.

Control register to configure PDR Kp loop controller gain setting for half-bridges 5-8.

Figure 8-51. PDR_CTRL10 Register

7	6	5	4	3	2	1	0
EN_PDR_56	PDR_ERR_56	KP_PDR_56		EN_PDR_78	PDR_ERR_78	KP_PDR_78	
R/W-0b	R/W-0b	R/W-01b		R/W-0b	R/W-0b	R/W-01b	

Table 8-61. PDR_CTRL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_PDR_56	R/W	0b	Enable PDR loop control for half-bridge 5 and 6.
6	PDR_ERR_56	R/W	0b	PDR loop error limit for half-bridge 5 and 6. 0b = 1-bit error 1b = Actual error
5-4	KP_PDR_56	R/W	01b	PDR proportional controller gain setting for half-bridge 5 and 6. 00b = 1 01b = 2 10b = 3 11b = 4
3	EN_PDR_78	R/W	0b	Enable PDR loop control for half-bridge 7 and 8.

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Table 8-61. PDR_CTRL10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PDR_ERR_78	R/W	0b	PDR loop error limit for half-bridge 7 and 8. 0b = 1-bit error 1b = Actual error
1-0	KP_PDR_78	R/W	01b	PDR proportional controller gain setting for half-bridge 7 and 8. 00b = 1 01b = 2 10b = 3 11b = 4

8.3.3.12 STC_CTRL1 Register (Address = 35h) [Reset = 23h]

STC_CTRL1 is shown in Figure 8-52 and described in Table 8-62.

Return to the Summary Table.

Control register to configure STC rise/fall time and Kp loop controller gain setting for half-bridges 1 and 2.

Figure 8-52. STC_CTRL1 Register

7	6	5	4	3	2	1	0
T_RISE_FALL_12				EN_STC_12	STC_ERR_12	KP_STC_12	
R/W-0010b				R/W-0b	R/W-0b	R/W-11b	

Table 8-62. STC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	T_RISE_FALL_12	R/W	0010b	Set switch-node VSH rise and fall time for half-bridge 1 and 2. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us
3	EN_STC_12	R/W	0b	Enable STC loop control for half-bridge 1 and 2.
2	STC_ERR_12	R/W	0b	STC loop error limit for half-bridge 1 and 2 0b = 1-bit error 1b = Actual error
1-0	KP_STC_12	R/W	11b	STC proportional controller gain setting for half-bridge 1 and 2. 00b = 1 01b = 2 10b = 3 11b = 4

8.3.3.13 STC_CTRL2 Register (Address = 36h) [Reset = 23h]

STC_CTRL2 is shown in Figure 8-53 and described in Table 8-63.

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Control register to configure STC rise/fall time and Kp loop controller gain setting for half-bridges 3 and 4.

Figure 8-53. STC_CTRL2 Register

7	6	5	4	3	2	1	0
T_RISE_FALL_34				EN_STC_34	STC_ERR_34	KP_STC_34	
R/W-0010b				R/W-0b	R/W-0b	R/W-11b	

Table 8-63. STC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	T_RISE_FALL_34	R/W	0010b	Set switch-node VSH rise and fall time for half-bridge 3 and 4. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us
3	EN_STC_34	R/W	0b	Enable STC loop control for half-bridge 3 and 4.
2	STC_ERR_34	R/W	0b	STC loop error limit for half-bridge 3 and 4. 0b = 1-bit error 1b = Actual error
1-0	KP_STC_34	R/W	11b	STC proportional controller gain setting for half-bridge 3 and 4. 00b = 1 01b = 2 10b = 3 11b = 4

8.3.3.14 STC_CTRL3 Register (Address = 37h) [Reset = 23h]

STC_CTRL3 is shown in Figure 8-54 and described in Table 8-64.

Return to the Summary Table.

Control register to configure STC rise/fall time and Kp loop controller gain setting for half-bridges 5 and 6.

Figure 8-54. STC_CTRL3 Register

7	6	5	4	3	2	1	0
T_RISE_FALL_56				EN_STC_56	STC_ERR_56	KP_STC_56	
R/W-0010b				R/W-0b	R/W-0b	R/W-11b	

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Table 8-64. STC_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	T_RISE_FALL_56	R/W	0010b	Set switch-node VSH rise and fall time for half-bridge 5 and 6. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us
3	EN_STC_56	R/W	0b	Enable STC loop control for half-bridge 5 and 6.
2	STC_ERR_56	R/W	0b	STC loop error limit for half-bridge 5 and 6. 0b = 1-bit error 1b = Actual error
1-0	KP_STC_56	R/W	11b	STC proportional controller gain setting for half-bridge 5 and 6. 00b = 1 01b = 2 10b = 3 11b = 4

8.3.3.15 STC_CTRL4 Register (Address = 38h) [Reset = 23h]

STC_CTRL4 is shown in Figure 8-55 and described in Table 8-65.

Return to the Summary Table.

Control register to configure STC rise/fall time and Kp loop controller gain setting for half-bridges 7 and 8.

Figure 8-55. STC_CTRL4 Register

7	6	5	4	3	2	1	0
T_RISE_FALL_78				EN_STC_78	STC_ERR_78	KP_STC_78	
R/W-0010b				R/W-0b	R/W-0b	R/W-11b	

Table 8-65. STC_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	T_RISE_FALL_78	R/W	0010b	Set switch-node VSH rise and fall time for half-bridge 7 and 8. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us

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Table 8-65. STC_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EN_STC_78	R/W	0b	Enable STC loop control for half-bridge 7 and 8.
2	STC_ERR_78	R/W	0b	STC loop error limit for half-bridge 7 and 8. 0b = 1-bit error 1b = Actual error
1-0	KP_STC_78	R/W	11b	STC proportional controller gain setting for half-bridge 7 and 8. 00b = 1 01b = 2 10b = 3 11b = 4

8.3.3.16 DCC_CTRL1 Register (Address = 39h) [Reset = 0h]

DCC_CTRL1 is shown in Figure 8-56 and described in Table 8-66.

Return to the Summary Table.

Control register to enable DCC loop and manual configuration for half-bridges 1-8.

Figure 8-56. DCC_CTRL1 Register

7	6	5	4	3	2	1	0
EN_DCC_12	EN_DCC_34	EN_DCC_56	EN_DCC_78	IDIR_MAN_12	IDIR_MAN_34	IDIR_MAN_56	IDIR_MAN_78
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-66. DCC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_DCC_12	R/W	0b	Enable duty cycle compensation for half-bridge 1 and 2.
6	EN_DCC_34	R/W	0b	Enable duty cycle compensation for half-bridge 3 and 4.
5	EN_DCC_56	R/W	0b	Enable duty cycle compensation for half-bridge 5 and 6.
4	EN_DCC_78	R/W	0b	Enable duty cycle compensation for half-bridge 7 and 8.
3	IDIR_MAN_12	R/W	0b	Current polarity detection mode for half-bridge 1 and 2. 0b = Automatic 1b = Manual (Set by HBx_HL)
2	IDIR_MAN_34	R/W	0b	Current polarity detection mode for half-bridge 3 and 4. 0b = Automatic 1b = Manual (Set by HBx_HL)
1	IDIR_MAN_56	R/W	0b	Current polarity detection mode for half-bridge 5 and 6. 0b = Automatic 1b = Manual (Set by HBx_HL)
0	IDIR_MAN_78	R/W	0b	Current polarity detection mode for half-bridge 7 and 8. 0b = Automatic 1b = Manual (Set by HBx_HL)

8.3.3.17 PST_CTRL1 Register (Address = 3Ah) [Reset = Fh]

PST_CTRL1 is shown in Figure 8-57 and described in Table 8-67.

Return to the Summary Table.

Control register to configure max freewheeling current and post charge delay for half-bridges 1-8.

Figure 8-57. PST_CTRL1 Register

7	6	5	4	3	2	1	0
FW_MAX_12	FW_MAX_34	FW_MAX_56	FW_MAX_78	EN_PST_DLY_12	EN_PST_DLY_34	EN_PST_DLY_56	EN_PST_DLY_78
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

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Figure 8-57. PST_CTRL1 Register (continued)

Table 8-67. PST_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FW_MAX_12	R/W	0b	Gate drive current used for freewheeling MOSFET for half-bridge 1 and 2. 0b = PRE_CHR_MAX_12 [1:0] 1b = 64 mA
6	FW_MAX_34	R/W	0b	Gate drive current used for freewheeling MOSFET for half-bridge 3 and 4. 0b = PRE_CHR_MAX_34 [1:0] 1b = 64 mA
5	FW_MAX_56	R/W	0b	Gate drive current used for freewheeling MOSFET for half-bridge 5 and 6. 0b = PRE_CHR_MAX_56 [1:0] 1b = 64 mA
4	FW_MAX_78	R/W	0b	Gate drive current used for freewheeling MOSFET for half-bridge 7 and 8. 0b = PRE_CHR_MAX_78 [1:0] 1b = 64 mA
3	EN_PST_DLY_12	R/W	1b	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_12 - T_PRE_CHR_12.
2	EN_PST_DLY_34	R/W	1b	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_34 - T_PRE_CHR_34.
1	EN_PST_DLY_56	R/W	1b	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_56 - T_PRE_CHR_56.
0	EN_PST_DLY_78	R/W	1b	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_78 - T_PRE_CHR_78.

8.3.3.18 PST_CTRL2 Register (Address = 3Bh) [Reset = 55h]

PST_CTRL2 is shown in Figure 8-58 and described in Table 8-68.

Return to the Summary Table.

Control register to configure post charge Kp loop controller gain setting for half-bridges 1-8.

Figure 8-58. PST_CTRL2 Register

7	6	5	4	3	2	1	0
KP_PST_12		KP_PST_34		KP_PST_56		KP_PST_78	
R/W-01b		R/W-01b		R/W-01b		R/W-01b	

Table 8-68. PST_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	KP_PST_12	R/W	01b	Post charge proportional control gain setting for half-bridges 1 and 2. 00b = Disabled 01b = 2 10b = 4 11b = 15
5-4	KP_PST_34	R/W	01b	Post charge proportional control gain setting for half-bridges 3 and 4. 00b = Disabled 01b = 2 10b = 4 11b = 15
3-2	KP_PST_56	R/W	01b	Post charge proportional control gain setting for half-bridges 5 and 6. 00b = Disabled 01b = 2 10b = 4 11b = 15

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Table 8-68. PST_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	KP_PST_78	R/W	01b	Post charge proportional control gain setting for half-bridges 7 and 8. 00b = Disabled 01b = 2 10b = 4 11b = 15

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8.3.4 DRV8718-Q1_STATUS_ADV Registers

Table 8-69 lists the DRV8718-Q1_STATUS_ADV registers. All register offset addresses not listed in Table 8-69 should be considered as reserved locations and the register contents should not be modified.

Table 8-69. DRV8718-Q1_STATUS_ADV Registers

Address	Acronym	Register Name	Section
3Ch	SGD_STAT1	Half-bridge 1-8 current polarity indicators	Go
3Dh	SGD_STAT2	Half-bridge 1-8 PDR underflow and overflow indicators	Go
3Eh	SGD_STAT3	Half-bridge 1-8 STC fault indicator	Go

Complex bit access types are encoded to fit into small table cells. Table 8-70 shows the codes that are used for access types in this section.

Table 8-70. DRV8718-Q1_STATUS_ADV Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
- *n*		Value after reset or the default value

8.3.4.1 SGD_STAT1 Register (Address = 3Ch) [Reset = 0h]

SGD_STAT1 is shown in Figure 8-59 and described in Table 8-71.

Return to the Summary Table.

Status registers indicating current polarity for half-bridges 1-8.

Figure 8-59. SGD_STAT1 Register

7	6	5	4	3	2	1	0
IDIR_12	IDIR_34	IDIR_56	IDIR_78	IDIR_WARN_12	IDIR_WARN_34	IDIR_WARN_56	IDIR_WARN_78
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-71. SGD_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IDIR_12	R	0b	Indicated current direction for half-bridge 1 and 2.
6	IDIR_34	R	0b	Indicated current direction for half-bridge 3 and 4.
5	IDIR_56	R	0b	Indicated current direction for half-bridge 5 and 6.
4	IDIR_78	R	0b	Indicated current direction for half-bridge 7 and 8.
3	IDIR_WARN_12	R	0b	Indicates unknown current direction for half-bridge 1 and 2.
2	IDIR_WARN_34	R	0b	Indicates unknown current direction for half-bridge 3 and 4.
1	IDIR_WARN_56	R	0b	Indicates unknown current direction for half-bridge 5 and 6.
0	IDIR_WARN_78	R	0b	Indicates unknown current direction for half-bridge 7 and 8.

8.3.4.2 SGD_STAT2 Register (Address = 3Dh) [Reset = 0h]

SGD_STAT2 is shown in Figure 8-60 and described in Table 8-72.

Return to the Summary Table.

Status registers indicating underflow and overflow in PDR loop control for half-bridges 1-8.

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Figure 8-60. SGD_STAT2 Register

7	6	5	4	3	2	1	0
PCHR_WARN_12	PCHR_WARN_34	PCHR_WARN_56	PCHR_WARN_78	PDCHR_WARN_12	PDCHR_WARN_34	PDCHR_WARN_56	PDCHR_WARN_78
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-72. SGD_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PCHR_WARN_12	R	0b	Indicates pre-charge underflow or overflow fault for half-bridge 1 and 2.
6	PCHR_WARN_34	R	0b	Indicates pre-charge underflow or overflow fault for half-bridge 3 and 4.
5	PCHR_WARN_56	R	0b	Indicates pre-charge underflow or overflow fault for half-bridge 5 and 6.
4	PCHR_WARN_78	R	0b	Indicates pre-charge underflow or overflow fault for half-bridge 7 and 8.
3	PDCHR_WARN_12	R	0b	Indicates pre-discharge underflow or overflow fault for half-bridge 1 and 2.
2	PDCHR_WARN_34	R	0b	Indicates pre-discharge underflow or overflow fault for half-bridge 3 and 4.
1	PDCHR_WARN_56	R	0b	Indicates pre-discharge underflow or overflow fault for half-bridge 5 and 6.
0	PDCHR_WARN_78	R	0b	Indicates pre-discharge underflow or overflow fault for half-bridge 7 and 8.

8.3.4.3 SGD_STAT3 Register (Address = 3Eh) [Reset = 0h]

SGD_STAT3 is shown in Figure 8-61 and described in Table 8-73.

Return to the Summary Table.

Status register indicator STC rise and fall time overflow for half-bridges 1-8.

Figure 8-61. SGD_STAT3 Register

7	6	5	4	3	2	1	0
STC_WARN_F_12	STC_WARN_F_34	STC_WARN_F_56	STC_WARN_F_78	STC_WARN_R_12	STC_WARN_R_34	STC_WARN_R_56	STC_WARN_R_78
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-73. SGD_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STC_WARN_F_12	R	0b	Indicates falling slew time TDRV overflow for half-bridge 1 and 2.
6	STC_WARN_F_34	R	0b	Indicates falling slew time TDRV overflow for half-bridge 3 and 4.
5	STC_WARN_F_56	R	0b	Indicates falling slew time TDRV overflow for half-bridge 5 and 6.
4	STC_WARN_F_78	R	0b	Indicates falling slew time TDRV overflow for half-bridge 7 and 8.
3	STC_WARN_R_12	R	0b	Indicates rising slew time TDRV overflow for half-bridge 1 and 2.
2	STC_WARN_R_34	R	0b	Indicates rising slew time TDRV overflow for half-bridge 3 and 4.
1	STC_WARN_R_56	R	0b	Indicates rising slew time TDRV overflow for half-bridge 5 and 6.
0	STC_WARN_R_78	R	0b	Indicates rising slew time TDRV overflow for half-bridge 7 and 8.

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8.4 DRV8714-Q1 Register Descriptions

8.4.1 DRV8714-Q1_STATUS Registers

Table 8-74 lists the DRV8714-Q1_STATUS registers. All register offset addresses not listed in Table 8-74 should be considered as reserved locations and the register contents should not be modified.

Table 8-74. DRV8714-Q1_STATUS Registers

Address	Acronym	Register Name	Section
0h	IC_STAT1	Global fault and warning status indicators	Go
1h	VDS_STAT1	Half-bridge 1-4 VDS overcurrent fault status indicators	Go
3h	VGS_STAT1	Half-bridge 1-4 VGS gate fault status indicators	Go
5h	IC_STAT2	Voltage, temperature and interface fault status indicators	Go
6h	IC_STAT3	Device variant ID status register	Go

Complex bit access types are encoded to fit into small table cells. Table 8-75 shows the codes that are used for access types in this section.

Table 8-75. DRV8714-Q1_STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
- *n*		Value after reset or the default value

8.4.1.1 IC_STAT1 Register (Address = 0h) [Reset = C0h]

IC_STAT1 is shown in Figure 8-62 and described in Table 8-76.

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Status register for global fault and warning indicators. Detailed fault information is available in remaining status registers.

Figure 8-62. IC_STAT1 Register

7	6	5	4	3	2	1	0
SPI_OK	POR	FAULT	WARN	DS_GS	UV	OV	OT_WD_AGD
R-1b	R-1b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-76. IC_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_OK	R	1b	Indicates if a SPI communications fault has been detected. 0b = One or multiple of SCLK_FLT in the prior frames. 1b = No SPI fault has been detected
6	POR	R	1b	Indicates power-on-reset condition. 0b = No power-on-reset condition detected. 1b = Power-on reset condition detected.
5	FAULT	R	0b	Fault indicator. Mirrors nFAULT pin.
4	WARN	R	0b	Warning indicator.
3	DS_GS	R	0b	Logic OR of VDS and VGS fault indicators.
2	UV	R	0b	Undervoltage indicator.
1	OV	R	0b	Overvoltage indicator.
0	OT_WD_AGD	R	0b	Logic OR of OTW, OTSD, WD_FLT, IDIR_WARN, PCHR_WARN, PDCHR_WARN, and STC_WARN indicators.

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8.4.1.2 VDS_STAT1 Register (Address = 1h) [Reset = 0h]

VDS_STAT1 is shown in Figure 8-63 and described in Table 8-77.

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Status register for the specific MOSFET VDS overcurrent fault indication for half-bridges 1-4.

Figure 8-63. VDS_STAT1 Register

7	6	5	4	3	2	1	0
VDS_H1	VDS_L1	VDS_H2	VDS_L2	VDS_H3	VDS_L3	VDS_H4	VDS_L4
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-77. VDS_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VDS_H1	R	0b	Indicates VDS overcurrent fault on the high-side 1 MOSFET.
6	VDS_L1	R	0b	Indicates VDS overcurrent fault on the low-side 1 MOSFET.
5	VDS_H2	R	0b	Indicates VDS overcurrent fault on the high-side 2 MOSFET.
4	VDS_L2	R	0b	Indicates VDS overcurrent fault on the low-side 2 MOSFET.
3	VDS_H3	R	0b	Indicates VDS overcurrent fault on the high-side 3 MOSFET.
2	VDS_L3	R	0b	Indicates VDS overcurrent fault on the low-side 3 MOSFET.
1	VDS_H4	R	0b	Indicates VDS overcurrent fault on the high-side 4 MOSFET.
0	VDS_L4	R	0b	Indicates VDS overcurrent fault on the low-side 4 MOSFET.

8.4.1.3 VGS_STAT1 Register (Address = 3h) [Reset = 0h]

VGS_STAT1 is shown in Figure 8-64 and described in Table 8-78.

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Status register for the specific MOSFET VGS gate fault indication for half-bridges 1-4.

Figure 8-64. VGS_STAT1 Register

7	6	5	4	3	2	1	0
VGS_H1	VGS_L1	VGS_H2	VGS_L2	VGS_H3	VGS_L3	VGS_H4	VGS_L4
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-78. VGS_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VGS_H1	R	0b	Indicates VGS gate fault on the high-side 1 MOSFET.
6	VGS_L1	R	0b	Indicates VGS gate fault on the low-side 1 MOSFET.
5	VGS_H2	R	0b	Indicates VGS gate fault on the high-side 2 MOSFET.
4	VGS_L2	R	0b	Indicates VGS gate fault on the low-side 2 MOSFET.
3	VGS_H3	R	0b	Indicates VGS gate fault on the high-side 3 MOSFET.
2	VGS_L3	R	0b	Indicates VGS gate fault on the low-side 3 MOSFET.
1	VGS_H4	R	0b	Indicates VGS gate fault on the high-side 4 MOSFET.
0	VGS_L4	R	0b	Indicates VGS gate fault on the low-side 4 MOSFET.

8.4.1.4 IC_STAT2 Register (Address = 5h) [Reset = 0h]

IC_STAT2 is shown in Figure 8-65 and described in Table 8-79.

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Status register for specific undervoltage, overvoltage, overtemperature, and interface fault indications.

Figure 8-65. IC_STAT2 Register

7	6	5	4	3	2	1	0
PVDD_UV	PVDD_OV	VCP_UV	OTW	OTSD	WD_FLT	SCLK_FLT	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-79. IC_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_UV	R	0b	Indicates undervoltage fault on PVDD pin.
6	PVDD_OV	R	0b	Indicates overvoltage fault on PVDD pin.
5	VCP_UV	R	0b	Indicates undervoltage fault on VCP pin.
4	OTW	R	0b	Indicates overtemperature warning.
3	OTSD	R	0b	Indicates overtemperature shutdown.
2	WD_FLT	R	0b	Indicated watchdog timer fault.
1	SCLK_FLT	R	0b	Indicates SPI clock (frame) fault when the number of SCLK pulses in a transaction frame are not equal to 16. Not reported on FAULT or nFAULT pin.
0	RESERVED	R	0b	Reserved

8.4.1.5 IC_STAT3 Register (Address = 6h) [Reset = 4h]

IC_STAT3 is shown in Figure 8-66 and described in Table 8-80.

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Status register with device ID for either DRV8718-Q1 or DRV8714-Q1.

Figure 8-66. IC_STAT3 Register

7	6	5	4	3	2	1	0
RESERVED				IC_ID			
R-0000b				R-0100b			

Table 8-80. IC_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved
3-0	IC_ID	R	0100b	Device identification field. 0100b = DRV8714-Q1, 4 half-bridge gate driver. 1000b = DRV8718-Q1, 8 half-bridge gate driver.

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8.4.2 DRV8714-Q1_CONTROL Registers

Table 8-81 lists the DRV8714-Q1_CONTROL registers. All register offset addresses not listed in Table 8-81 should be considered as reserved locations and the register contents should not be modified.

Table 8-81. DRV8714-Q1_CONTROL Registers

Address	Acronym	Register Name	Section
7h	IC_CTRL1	Device general function control register 1	Go
8h	IC_CTRL2	Device general function control register 2	Go
9h	BRG_CTRL1	Half-bridge 1-4 output state control	Go
Ah	BRG_CTRL2	H-bridge 1/2 and 3/4 control	Go
Bh	PWM_CTRL1	Half-bridge 1-4 PWM mapping control	Go
Ch	PWM_CTRL2	H-bridge 1/2 and 3/4 configuration	Go
Dh	PWM_CTRL3	Half-bridge 1-4 high-side or low-side drive control	Go
Eh	PWM_CTRL4	Half-bridge 1-4 freewheeling configuration	Go
Fh	IDRV_CTRL1	Half-bridge 1 gate drive source/sink current	Go
10h	IDRV_CTRL2	Half-bridge 2 gate drive source/sink current	Go
11h	IDRV_CTRL3	Half-bridge 3 gate drive source/sink current	Go
12h	IDRV_CTRL4	Half-bridge 4 gate drive source/sink current	Go
17h	IDRV_CTRL9	Half-bridge 1-4 gate drive low current control	Go
18h	DRV_CTRL1	Gate driver VGS and VDS monitor configuration	Go
19h	DRV_CTRL2	Half-bridge 1 and 2 VGS and VDS tDRV configuration	Go
1Ah	DRV_CTRL3	Half-bridge 3 and 4 VGS and VDS tDRV configuration	Go
1Bh	DRV_CTRL4	Half-bridge 1-4 VGS tDEAD_D configuration	Go
1Ch	DRV_CTRL5	Half-bridge 1-4 VDS tDS_DG configuration	Go
1Dh	DRV_CTRL6	Half-bridge 1-4 VDS fault pulldown current configuration	Go
1Fh	VDS_CTRL1	Half-bridge 1 and 2 VDS overcurrent threshold	Go
20h	VDS_CTRL2	Half-bridge 3 and 4 VDS overcurrent threshold	Go
23h	OLSC_CTRL1	Half-bridge 1-4 offline diagnostic control	Go
25h	UVOV_CTRL	Undervoltage and overvoltage monitor configuration.	Go
26h	CSA_CTRL1	Shunt amplifier 1 and 2 configuration	Go
27h	CSA_CTRL2	Shunt amplifier 1 blanking configuration	Go
28h	CSA_CTRL3	Shunt amplifier 2 blanking configuration	Go

Complex bit access types are encoded to fit into small table cells. Table 8-82 shows the codes that are used for access types in this section.

Table 8-82. DRV8714-Q1_CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
- *n*		Value after reset or the default value

8.4.2.1 IC_CTRL1 Register (Address = 7h) [Reset = 6h]

IC_CTRL1 is shown in Figure 8-67 and described in Table 8-83.

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Control register for driver and diagnostic enable, PWM control mode, SPI lock, and clear fault command.

Figure 8-67. IC_CTRL1 Register

7	6	5	4	3	2	1	0
EN_DRV	EN_OLSC	BRG_MODE		LOCK			CLR_FLT
R/W-0b	R/W-0b	R/W-00b		R/W-011b			R/W-0b

Table 8-83. IC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_DRV	R/W	0b	Enable gate drivers. 0b = Gate driver output disabled and passive pulldowns enabled. 1b = Gate driver outputs enabled.
6	EN_OLSC	R/W	0b	Enable offline open load and short circuit diagnostic. 0b = Disabled. 1b = VDS monitors set into real-time voltage monitor mode and offline diagnostics current sources enabled.
5-4	BRG_MODE	R/W	00b	Bridge PWM control mode. 00b = Independent Half-Bridge 01b = H-Bridge PH/EN 10b = H-Bridge PWM 11b = Solenoid Control
3-1	LOCK	R/W	011b	Lock and unlock the control registers. Bit settings not listed have no effect. 011b = Unlock all control registers. 110b = Lock the control registers by ignoring further writes except to the LOCK register.
0	CLR_FLT	R/W	0b	Clear latched fault status information. 0b = Default state. 1b = Clear latched fault bits, resets to 0b after completion. Will also clear SPI fault and watchdog fault status.

8.4.2.2 IC_CTRL2 Register (Address = 8h) [Reset = 2h]

IC_CTRL2 is shown in Figure 8-68 and described in Table 8-84.

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Control register for pin mode, charge pump mode, and watchdog.

Figure 8-68. IC_CTRL2 Register

7	6	5	4	3	2	1	0
DIS_SSC	DRVOFF_nFLT	CP_MODE		WD_EN	WD_FLT_M	WD_WIN	WD_RST
R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-1b	R/W-0b

Table 8-84. IC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIS_SSC	R/W	0b	Spread spectrum clocking 0b = Enabled. 1b = Disabled.
6	DRVOFF_nFLT	R/W	0b	Sets DRVOFF/nFLT multi-function pin mode. 0b = Pin functions as DRVOFF global driver disable. 1b = Pin functions as nFLT open-drain fault interrupt output.

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Table 8-84. IC_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	CP_MODE	R/W	00b	Charge pump operating mode. 00b = Automatic switch between tripler and doubler mode. 01b = Always doubler mode. 10b = Always tripler mode. 11b = RSVD
3	WD_EN	R/W	0b	Watchdog timer enable. 0b = Watchdog timer disabled. 1b = Watchdog dog timer enabled.
2	WD_FLT_M	R/W	0b	Watchdog fault mode. Watchdog fault is cleared by CLR_FLT. 0b = Watchdog fault is reported to WD_FLT and WARN register bits. Gate drivers remain enabled and nFAULT is not asserted. 1b = Watchdog fault is reported to WD_FLT, FAULT register bits, and nFAULT pin. Gate drivers are disabled in response to watchdog fault.
1	WD_WIN	R/W	1b	Watchdog timer window. 0b = 4 to 40 ms 1b = 10 to 100 ms
0	WD_RST	R/W	0b	Watchdog restart. 0b by default after power up. Invert this bit to restart the watchdog timer. After written, the bit will reflect the new inverted value.

8.4.2.3 BRG_CTRL1 Register (Address = 9h) [Reset = 0h]

BRG_CTRL1 is shown in Figure 8-69 and described in Table 8-85.

Return to the Summary Table.

Control register to set the output state for half-bridges 1-4 in independent half-bridge mode (BRG_MODE = 00b).

Figure 8-69. BRG_CTRL1 Register

7	6	5	4	3	2	1	0
HB1_CTRL		HB2_CTRL		HB3_CTRL		HB4_CTRL	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-85. BRG_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HB1_CTRL	R/W	00b	Half-bridge 1 output state control. 00b = High impedance (HI-Z). GH1 and GL1 pulldown. 01b = Drive low-side (LO). GH1 pulldown and GL1 pullup. 10b = Drive high-side (HI). GH1 pullup and GL1 pulldown. 11b = Input PWM control. HB1_PWM, HB1_HL, and HB1_FW.
5-4	HB2_CTRL	R/W	00b	Half-bridge 2 output state control. 00b = High impedance (HI-Z). GH2 and GL2 pulldown. 01b = Drive low-side (LO). GH2 pulldown and GL2 pullup. 10b = Drive high-side (HI). GH2 pullup and GL2 pulldown. 11b = Input PWM control. HB2_PWM, HB2_HL, and HB2_FW.
3-2	HB3_CTRL	R/W	00b	Half-bridge 3 output state control. 00b = High impedance (HI-Z). GH3 and GL3 pulldown. 01b = Drive low-side (LO). GH3 pulldown and GL3 pullup. 10b = Drive high-side (HI). GH3 pullup and GL3 pulldown. 11b = Input PWM control. HB3_PWM, HB3_HL, and HB3_FW.
1-0	HB4_CTRL	R/W	00b	Half-bridge 4 output state control. 00b = High impedance (HI-Z). GH4 and GL4 pulldown. 01b = Drive low-side (LO). GH4 pulldown and GL4 pullup. 10b = Drive high-side (HI). GH4 pullup and GL4 pulldown. 11b = Input PWM control. HB4_PWM, HB4_HL, and HB4_FW.

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8.4.2.4 BRG_CTRL2 Register (Address = Ah) [Reset = 0h]

BRG_CTRL2 is shown in Figure 8-70 and described in Table 8-86.

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Control register to set the output state for H-bridges 1/2 and 3/4 in H-bridge control modes (BRG_MODE = 01b, 10b, or 11b)

Figure 8-70. BRG_CTRL2 Register

7	6	5	4	3	2	1	0
S_IN1/EN1	S_IN2/PH1	HIZ1	RESERVED	S_IN3/EN2	S_IN4/PH2	HIZ2	RESERVED
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R-0b

Table 8-86. BRG_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	S_IN1/EN1	R/W	0b	Control bit for IN1/EN1 input signal. Enabled through IN1/EN1_MODE bit.
6	S_IN2/PH1	R/W	0b	Control bit for IN2/PH1 input signal. Enabled through IN2/PH1_MODE bit.
5	HIZ1	R/W	0b	Control bit for HIZ1 input signal. 0b = Outputs follow IN1/EN1 and IN2/PH1 signals. 1b = Gate drivers pulldowns are enabled. Half-bridges 1 and 2 Hi-Z
4	RESERVED	R	0b	Reserved
3	S_IN3/EN2	R/W	0b	Control bit for IN3/EN2 input signal. Enabled through IN3/EN2_MODE bit.
2	S_IN4/PH2	R/W	0b	Control bit for IN4/PH2 input signal. Enabled through IN4/PH2_MODE bit.
1	HIZ2	R/W	0b	Control bit for HIZ2 input signal. 0b = Outputs follow IN3/EN2 and IN4/PH2 signals. 1b = Gate drivers pulldowns are enabled. Half-bridges 3 and 4 Hi-Z
0	RESERVED	R	0b	Reserved

8.4.2.5 PWM_CTRL1 Register (Address = Bh) [Reset = 5h]

PWM_CTRL1 is shown in Figure 8-71 and described in Table 8-87.

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Control register to map the input PWM source for half-bridges 1-4 in independent half-bridge mode (BRG_MODE = 00b).

Figure 8-71. PWM_CTRL1 Register

7	6	5	4	3	2	1	0
HB1_PWM		HB2_PWM		HB3_PWM		HB4_PWM	
R/W-00b		R/W-00b		R/W-01b		R/W-01b	

Table 8-87. PWM_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HB1_PWM	R/W	00b	Configure PWM input source for half-bridge 1. 00b = IN1 01b = IN2 10b = IN3 11b = IN4

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Table 8-87. PWM_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	HB2_PWM	R/W	00b	Configure PWM input source for half-bridge 2. 00b = IN1 01b = IN2 10b = IN3 11b = IN4
3-2	HB3_PWM	R/W	01b	Configure PWM input source for half-bridge 3. 00b = IN1 01b = IN2 10b = IN3 11b = IN4
1-0	HB4_PWM	R/W	01b	Configure PWM input source for half-bridge 4. 00b = IN1 01b = IN2 10b = IN3 11b = IN4

8.4.2.6 PWM_CTRL2 Register (Address = Ch) [Reset = 0h]

PWM_CTRL2 is shown in Figure 8-72 and described in Table 8-88.

Return to the Summary Table.

Control register to configure the PWM method for H-bridges 1/2 and 3/4 in H-bridge control modes (BRG_MODE = 01b, 10b, or 11b)

Figure 8-72. PWM_CTRL2 Register

7	6	5	4	3	2	1	0
IN1/ EN1_MODE	IN2/ PH1_MODE	FW1	RESERVED	IN3/ EN2_MODE	IN4/ PH2_MODE	FW2	RESERVED
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R-0b

Table 8-88. PWM_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN1/EN1_MODE	R/W	0b	IN1/EN1 control mode. 0b = IN1/EN1 signal is sourced from the IN1/EN1 pin. 1b = IN1/EN1 signal is sourced from the S_IN1/EN1 bit.
6	IN2/PH1_MODE	R/W	0b	IN2/PH1 control mode. 0b = IN2/PH1 signal is sourced from the IN2/PH1 pin. 1b = IN2/PH1 signal is sourced from the S_IN2/PH1 bit.
5	FW1	R/W	0b	H-bridge 1 control freewheeling setting. 0b = Low-side freewheeling. 1b = High-side freewheeling.
4	RESERVED	R	0b	Reserved
3	IN3/EN2_MODE	R/W	0b	IN3/EN2 control mode. 0b = IN3/EN2 signal is sourced from the IN3/EN2 pin. 1b = IN3/EN2 signal is sourced from the S_IN3/EN2 bit.
2	IN4/PH2_MODE	R/W	0b	IN4/PH2 control mode. 0b = IN4/PH2 signal is sourced from the IN4/PH2 pin. 1b = IN4/PH2 signal is sourced from the S_IN4/PH2 bit.
1	FW2	R/W	0b	H-bridge 2 control freewheeling setting. 0b = Low-side freewheeling. 1b = High-side freewheeling.
0	RESERVED	R	0b	Reserved

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8.4.2.7 PWM_CTRL3 Register (Address = Dh) [Reset = 0h]

PWM_CTRL3 is shown in Figure 8-73 and described in Table 8-89.

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Control register to set the PWM drive MOSFET (high or low) for half-bridges 1-4.

Figure 8-73. PWM_CTRL3 Register

7	6	5	4	3	2	1	0
HB1_HL	HB2_HL	HB3_HL	HB4_HL	RESERVED			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0000b			

Table 8-89. PWM_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HB1_HL	R/W	0b	Map half-bridge 1 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
6	HB2_HL	R/W	0b	Map half-bridge 2 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
5	HB3_HL	R/W	0b	Map half-bridge 3 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
4	HB4_HL	R/W	0b	Map half-bridge 4 PWM to high-side or low-side gate driver. 0b = Set high-side as drive MOSFET. 1b = Set low-side as drive MOSFET.
3-0	RESERVED	R	0000b	Reserved

8.4.2.8 PWM_CTRL4 Register (Address = Eh) [Reset = 0h]

PWM_CTRL4 is shown in Figure 8-74 and described in Table 8-90.

Return to the Summary Table.

Control register to set the PWM freewheeling mode for half-bridges 1-4.

Figure 8-74. PWM_CTRL4 Register

7	6	5	4	3	2	1	0
HB1_FW	HB2_FW	HB3_FW	HB4_FW	RESERVED			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0000b			

Table 8-90. PWM_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HB1_FW	R/W	0b	Configure freewheeling setting for half-bridge 1. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
6	HB2_FW	R/W	0b	Configure freewheeling setting for half-bridge 2. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
5	HB3_FW	R/W	0b	Configure freewheeling setting for half-bridge 3. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
4	HB4_FW	R/W	0b	Configure freewheeling setting for half-bridge 4. 0b = Active. Generate inverted PWM internally. 1b = Passive. Rely on freewheeling diode.
3-0	RESERVED	R	0000b	Reserved

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8.4.2.9 IDRV_CTRL1 Register (Address = Fh) [Reset = FFh]

IDRV_CTRL1 is shown in Figure 8-75 and described in Table 8-91.

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Control register to configure the source and sink current for the half-bridge 1 high-side and low-side gate drivers.

Figure 8-75. IDRV_CTRL1 Register

7	6	5	4	3	2	1	0
IDRVP_1				IDRVN_1			
R/W-1111b				R/W-1111b			

Table 8-91. IDRV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_1	R/W	1111b	Half-bridge 1 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO1). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)
3-0	IDRVN_1	R/W	1111b	Half-bridge 1 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO1). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.4.2.10 IDRV_CTRL2 Register (Address = 10h) [Reset = FFh]

IDRV_CTRL2 is shown in Figure 8-76 and described in Table 8-92.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 2 high-side and low-side gate drivers.

Figure 8-76. IDRV_CTRL2 Register

7	6	5	4	3	2	1	0
IDRVP_2				IDRVN_2			

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Figure 8-76. IDRV_CTRL2 Register (continued)

R/W-1111b	R/W-1111b

Table 8-92. IDRV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_2	R/W	1111b	Half-bridge 2 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO2). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)
3-0	IDRVN_2	R/W	1111b	Half-bridge 2 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO2). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.4.2.11 IDRV_CTRL3 Register (Address = 11h) [Reset = FFh]

IDRV_CTRL3 is shown in Figure 8-77 and described in Table 8-93.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 3 high-side and low-side gate drivers.

Figure 8-77. IDRV_CTRL3 Register

7	6	5	4	3	2	1	0
IDRVP_3				IDRVN_3			
R/W-1111b				R/W-1111b			

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Table 8-93. IDRV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_3	R/W	1111b	Half-bridge 3 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO3). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)
3-0	IDRVN_3	R/W	1111b	Half-bridge 3 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO3). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.4.2.12 IDRV_CTRL4 Register (Address = 12h) [Reset = FFh]

IDRV_CTRL4 is shown in Figure 8-78 and described in Table 8-94.

Return to the Summary Table.

Control register to configure the source and sink current for the half-bridge 4 high-side and low-side gate drivers.

Figure 8-78. IDRV_CTRL4 Register

7	6	5	4	3	2	1	0
IDRVP_4				IDRVN_4			
R/W-1111b				R/W-1111b			

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Table 8-94. IDRV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	IDRVP_4	R/W	1111b	Half-bridge 4 peak source pull up current. Alternative low current value in parenthesis (IDRV_LO4). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)
3-0	IDRVN_4	R/W	1111b	Half-bridge 4 peak sink pull down current. Alternative low current value in parenthesis (IDRV_LO4). 0000b = 0.5 mA (50 µA) 0001b = 1 mA (110 µA) 0010b = 2 mA (170 µA) 0011b = 3 mA (230 µA) 0100b = 4 mA (290 µA) 0101b = 5 mA (350 µA) 0110b = 6 mA (410 µA) 0111b = 7 mA (600 µA) 1000b = 8 mA (725 µA) 1001b = 12 mA (850 µA) 1010b = 16 mA (1 mA) 1011b = 20 mA (1.2 mA) 1100b = 24 mA (1.4 mA) 1101b = 31 mA (1.6 mA) 1110b = 48 mA (1.8 mA) 1111b = 62 mA (2.3 mA)

8.4.2.13 IDRV_CTRL9 Register (Address = 17h) [Reset = 0h]

IDRV_CTRL9 is shown in Figure 8-79 and described in Table 8-95.

Return to the Summary Table.

Control register to enable ultra-low source and sink current settings for half-bridges 1-4.

Figure 8-79. IDRV_CTRL9 Register

7	6	5	4	3	2	1	0
IDRV_LO1	IDRV_LO2	IDRV_LO3	IDRV_LO4	RESERVED			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0000b			

Table 8-95. IDRV_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IDRV_LO1	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 1. 0b = IDRVP_1 and IDRVN_1 utilize standard values. 1b = IDRVP_1 and IDRVN_1 utilize low current values.
6	IDRV_LO2	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 2. 0b = IDRVP_2 and IDRVN_2 utilize standard values. 1b = IDRVP_2 and IDRVN_2 utilize low current values.

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Table 8-95. IDRV_CTRL9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	IDRV_LO3	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 3. 0b = IDRVP_3 and IDRVN_3 utilize standard values. 1b = IDRVP_3 and IDRVN_3 utilize low current values.
4	IDRV_LO4	R/W	0b	Enable low current IDRVN and IDRVP mode for half-bridge 4. 0b = IDRVP_4 and IDRVN_4 utilize standard values. 1b = IDRVP_4 and IDRVN_4 utilize low current values.
3-0	RESERVED	R	0000b	Reserved

8.4.2.14 DRV_CTRL1 Register (Address = 18h) [Reset = 0h]

DRV_CTRL1 is shown in Figure 8-80 and described in Table 8-96.

Return to the Summary Table.

Control register to set the VGS and VDS monitor operating modes and configurations.

Figure 8-80. DRV_CTRL1 Register

7	6	5	4	3	2	1	0
VGS_MODE		VGS_IND	VGS_LVL	VGS_HS_DIS	VDS_MODE		VDS_IND
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b

Table 8-96. DRV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VGS_MODE	R/W	00b	VGS gate fault monitor mode for half-bridges 1-4. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
5	VGS_IND	R/W	0b	VGS fault independent shutdown mode configuration. 0b = Disabled. VGS fault will shut down all half-bridge drivers. 1b = Enabled. VGS gate fault will only shutdown the associated half-bridge or H-bridge driver depending on BRG_MODE.
4	VGS_LVL	R/W	0b	VGS threshold comparator level for dead-time handshake and VGS fault monitor for half-bridge drivers. 0b = 1.4 V 1b = 1 V
3	VGS_HS_DIS	R/W	0b	VGS dead-time handshake monitor disable. 0b = 0x0 1b = Disabled. Half-bridge transition is based only on TDRIVE and programmable digital dead-time delays.
2-1	VDS_MODE	R/W	00b	VDS overcurrent monitor mode for half-bridges 1-4. 00b = Latched fault. 01b = Cycle by cycle. 10b = Warning report only. 11b = Disabled.
0	VDS_IND	R/W	0b	VDS fault independent shutdown mode configuration. 0b = Disabled. VDS fault will shut down all half-bridge drivers. 1b = Enabled. VDS gate fault will only shutdown the associated half-bridge or H-bridge drivers depending on BRG_MODE.

8.4.2.15 DRV_CTRL2 Register (Address = 19h) [Reset = 12h]

DRV_CTRL2 is shown in Figure 8-81 and described in Table 8-97.

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Control register to set tDRV, the VGS drive and VDS monitor blanking time for half-bridges 1 and 2.

Figure 8-81. DRV_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED		VGS_TDRV_1			VGS_TDRV_2		
R-00b		R/W-010b			R/W-010b		

Table 8-97. DRV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-3	VGS_TDRV_1	R/W	010b	VGS drive and VDS monitor blanking time for half-bridge 1. 000b = 2 µs 001b = 4 µs 010b = 8 µs 011b = 12 µs 100b = 16 µs 101b = 24 µs 110b = 32 µs 111b = 96 µs
2-0	VGS_TDRV_2	R/W	010b	VGS drive and VDS monitor blanking time for half-bridge 2. 000b = 2 µs 001b = 4 µs 010b = 8 µs 011b = 12 µs 100b = 16 µs 101b = 24 µs 110b = 32 µs 111b = 96 µs

8.4.2.16 DRV_CTRL3 Register (Address = 1Ah) [Reset = 12h]

DRV_CTRL3 is shown in Figure 8-82 and described in Table 8-98.

Return to the Summary Table.

Control register to set tDRV, the VGS drive and VDS monitor blanking time for half-bridges 3 and 4.

Figure 8-82. DRV_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		VGS_TDRV_3			VGS_TDRV_4		
R-00b		R/W-010b			R/W-010b		

Table 8-98. DRV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-3	VGS_TDRV_3	R/W	010b	VGS drive and VDS monitor blanking time for half-bridge 3. 000b = 2 µs 001b = 4 µs 010b = 8 µs 011b = 12 µs 100b = 16 µs 101b = 24 µs 110b = 32 µs 111b = 96 µs

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Table 8-98. DRV_CTRL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	VGS_TDRV_4	R/W	010b	VGS drive and VDS monitor blanking time for half-bridge 4. 000b = 2 µs 001b = 4 µs 010b = 8 µs 011b = 12 µs 100b = 16 µs 101b = 24 µs 110b = 32 µs 111b = 96 µs

8.4.2.17 DRV_CTRL4 Register (Address = 1Bh) [Reset = 0h]

DRV_CTRL4 is shown in Figure 8-83 and described in Table 8-99.

Return to the Summary Table.

Control register to set VGS tDEAD_D, additional digital dead-time insertion for half-bridges 1-4.

Figure 8-83. DRV_CTRL4 Register

7	6	5	4	3	2	1	0
VGS_TDEAD_1		VGS_TDEAD_2		VGS_TDEAD_3		VGS_TDEAD_4	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-99. DRV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VGS_TDEAD_1	R/W	00b	Insertable digital dead-time for half-bridge 1. 00b = 0 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
5-4	VGS_TDEAD_2	R/W	00b	Insertable digital dead-time for half-bridge 2. 00b = 0 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
3-2	VGS_TDEAD_3	R/W	00b	Insertable digital dead-time for half-bridge 3. 00b = 0 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
1-0	VGS_TDEAD_4	R/W	00b	Insertable digital dead-time for half-bridge 4. 00b = 0 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs

8.4.2.18 DRV_CTRL5 Register (Address = 1Ch) [Reset = AAh]

DRV_CTRL5 is shown in Figure 8-84 and described in Table 8-100.

Return to the Summary Table.

Control register to set VDS tDS_DG, overcurrent monitor deglitch time for half-bridges 1-4.

Figure 8-84. DRV_CTRL5 Register

7	6	5	4	3	2	1	0
VDS_DG_1		VDS_DG_2		VDS_DG_3		VDS_DG_4	

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Figure 8-84. DRV_CTRL5 Register (continued)

R/W-10b	R/W-10b	R/W-10b	R/W-10b

Table 8-100. DRV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VDS_DG_1	R/W	10b	VDS overcurrent monitor deglitch time for half-bridge 1. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
5-4	VDS_DG_2	R/W	10b	VDS overcurrent monitor deglitch time for half-bridge 2. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
3-2	VDS_DG_3	R/W	10b	VDS overcurrent monitor deglitch time for half-bridge 3. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
1-0	VDS_DG_4	R/W	10b	VDS overcurrent monitor deglitch time for half-bridge 4. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs

8.4.2.19 DRV_CTRL6 Register (Address = 1Dh) [Reset = 0h]

DRV_CTRL6 is shown in Figure 8-85 and described in Table 8-101.

Return to the Summary Table.

Control register to set the gate pulldown current (IDRVN) in response to VDS overcurrent fault for half-bridges 1-4.

Figure 8-85. DRV_CTRL6 Register

7	6	5	4	3	2	1	0
VDS_IDRVN_1		VDS_IDRVN_2		VDS_IDRVN_3		VDS_IDRVN_4	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-101. DRV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	VDS_IDRVN_1	R/W	00b	IDRVN gate pulldown current after VDS_OCP fault for half-bridge 1. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA
5-4	VDS_IDRVN_2	R/W	00b	IDRVN gate pulldown current after VDS_OCP fault for half-bridge 2. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA
3-2	VDS_IDRVN_3	R/W	00b	IDRVN gate pulldown current after VDS_OCP fault for half-bridge 3. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA

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Table 8-101. DRV_CTRL6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	VDS_IDRVN_4	R/W	00b	IDRVN gate pulldown current after VDS_OCP fault for half-bridge 4. 00b = Programmed IDRVN 01b = 8 mA 10b = 31 mA 11b = 62 mA

8.4.2.20 VDS_CTRL1 Register (Address = 1Fh) [Reset = DDh]

VDS_CTRL1 is shown in Figure 8-86 and described in Table 8-102.

Return to the Summary Table.

Control register to set the VDS overcurrent monitor voltage threshold for half-bridges 1 and 2.

Figure 8-86. VDS_CTRL1 Register

7	6	5	4	3	2	1	0
VDS_LVL_1				VDS_LVL_2			
R/W-1101b				R/W-1101b			

Table 8-102. VDS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	VDS_LVL_1	R/W	1101b	Half-bridge 1 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V
3-0	VDS_LVL_2	R/W	1101b	Half-bridge 2 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

8.4.2.21 VDS_CTRL2 Register (Address = 20h) [Reset = DDh]

VDS_CTRL2 is shown in Figure 8-87 and described in Table 8-103.

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Return to the Summary Table.

Control register to set the VDS overcurrent monitor voltage threshold for half-bridges 3 and 4.

Figure 8-87. VDS_CTRL2 Register

7	6	5	4	3	2	1	0
VDS_LVL_3				VDS_LVL_4			
R/W-1101b				R/W-1101b			

Table 8-103. VDS_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	VDS_LVL_3	R/W	1101b	Half-bridge 3 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V
3-0	VDS_LVL_4	R/W	1101b	Half-bridge 4 VDS overcurrent monitor threshold. 0000b = 0.06 V 0001b = 0.08 V 0010b = 0.10 V 0011b = 0.12 V 0100b = 0.14 V 0101b = 0.16 V 0110b = 0.18 V 0111b = 0.2 V 1000b = 0.3 V 1001b = 0.4 V 1010b = 0.5 V 1011b = 0.6 V 1100b = 0.7 V 1101b = 1 V 1110b = 1.4 V 1111b = 2 V

8.4.2.22 OLSC_CTRL1 Register (Address = 23h) [Reset = 0h]

OLSC_CTRL1 is shown in Figure 8-88 and described in Table 8-104.

Return to the Summary Table.

Control register to enable and disable the offline diagnostic current sources for half-bridges 1-4.

Figure 8-88. OLSC_CTRL1 Register

7	6	5	4	3	2	1	0
PU_SH1	PD_SH1	PU_SH2	PD_SH2	PU_SH3	PD_SH3	PU_SH4	PD_SH4
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

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Table 8-104. OLSC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PU_SH1	R/W	0b	Half-bridge 1 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
6	PD_SH1	R/W	0b	Half-bridge 1 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
5	PU_SH2	R/W	0b	Half-bridge 2 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
4	PD_SH2	R/W	0b	Half-bridge 2 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
3	PU_SH3	R/W	0b	Half-bridge 3 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
2	PD_SH3	R/W	0b	Half-bridge 3 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
1	PU_SH4	R/W	0b	Half-bridge 4 pull up diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.
0	PD_SH4	R/W	0b	Half-bridge 4 pull down diagnostic current source. Set EN_OLSC = 1b to use. 0b = Disabled. 1b = Enabled.

8.4.2.23 UVOV_CTRL Register (Address = 25h) [Reset = 14h]

UVOV_CTRL is shown in Figure 8-89 and described in Table 8-105.

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Control register to set the undervoltage and overvoltage monitor configurations.

Figure 8-89. UVOV_CTRL Register

7	6	5	4	3	2	1	0
PVDD_UV_MODE	PVDD_OV_MODE		PVDD_OV_DG		PVDD_OV_LVL	VCP_UV_MODE	VCP_UV_LVL
R/W-0b	R/W-00b		R/W-10b		R/W-1b	R/W-0b	R/W-0b

Table 8-105. UVOV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_UV_MODE	R/W	0b	PVDD supply undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
6-5	PVDD_OV_MODE	R/W	00b	PVDD supply overvoltage monitor mode. 00b = Latched fault. 01b = Automatic recovery. 10b = Warning report only. 11b = Disabled.

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Table 8-105. UVOV_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	PVDD_OV_DG	R/W	10b	PVDD supply overvoltage monitor deglitch time. 00b = 1 µs 01b = 2 µs 10b = 4 µs 11b = 8 µs
2	PVDD_OV_LVL	R/W	1b	PVDD supply overvoltage monitor threshold. 0b = 21.5 V 1b = 28.5 V
1	VCP_UV_MODE	R/W	0b	VCP charge pump undervoltage monitor mode. 0b = Latched fault. 1b = Automatic recovery.
0	VCP_UV_LVL	R/W	0b	VCP charge pump undervoltage monitor threshold. 0b = 4.75 V 1b = 6.25 V

8.4.2.24 CSA_CTRL1 Register (Address = 26h) [Reset = 9h]

CSA_CTRL1 is shown in Figure 8-90 and described in Table 8-106.

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Control register for gain and reference voltage for shunt amplifier 1 and 2.

Figure 8-90. CSA_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED		CSA_DIV_1	CSA_GAIN_1		CSA_DIV_2	CSA_GAIN_2	
R-00b		R/W-0b	R/W-01b		R/W-0b	R/W-01b	

Table 8-106. CSA_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5	CSA_DIV_1	R/W	0b	Current shunt amplifier 1 reference voltage divider. 0b = AREF / 2 1b = AREF / 8
4-3	CSA_GAIN_1	R/W	01b	Current shunt amplifier 1 gain setting. 00b = 10 V/V 01b = 20 V/V 10b = 40 V/V 11b = 80 V/V
2	CSA_DIV_2	R/W	0b	Current shunt amplifier 2 reference voltage divider. 0b = AREF / 2 1b = AREF / 8
1-0	CSA_GAIN_2	R/W	01b	Current shunt amplifier 2 gain setting. 00b = 10 V/V 01b = 20 V/V 10b = 40 V/V 11b = 80 V/V

8.4.2.25 CSA_CTRL2 Register (Address = 27h) [Reset = 0h]

CSA_CTRL2 is shown in Figure 8-91 and described in Table 8-107.

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Control register for shunt amplifier 1 blanking configuration.

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Figure 8-91. CSA_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED		CSA_BLK_SEL_1			CSA_BLK_LVL_1		
R-00b		R/W-000b			R/W-000b		

Table 8-107. CSA_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-3	CSA_BLK_SEL_1	R/W	000b	Current shunt amplifier 1 blanking trigger source. 000b = Half-bridge 1 001b = Half-bridge 2 010b = Half-bridge 3 011b = Half-bridge 4 100b = Half-bridge 5 101b = Half-bridge 6 110b = Half-bridge 7 111b = Half-bridge 8
2-0	CSA_BLK_LVL_1	R/W	000b	Current shunt amplifier 1 blanking time. % of tDRV. 000b = 0 %, Disabled 001b = 25 % 010b = 37.5 % 011b = 50 % 100b = 62.5 % 101b = 75 % 110b = 87.5 % 111b = 100 %

8.4.2.26 CSA_CTRL3 Register (Address = 28h) [Reset = 20h]

CSA_CTRL3 is shown in Figure 8-92 and described in Table 8-108.

Return to the Summary Table.

Control register for shunt amplifier 2 blanking configuration.

Figure 8-92. CSA_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		CSA_BLK_SEL_2			CSA_BLK_LVL_2		
R-00b		R/W-100b			R/W-000b		

Table 8-108. CSA_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved
5-3	CSA_BLK_SEL_2	R/W	100b	Current shunt amplifier 2 blanking trigger source. 000b = Half-bridge 1 001b = Half-bridge 2 010b = Half-bridge 3 011b = Half-bridge 4 100b = Half-bridge 5 101b = Half-bridge 6 110b = Half-bridge 7 111b = Half-bridge 8

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Table 8-108. CSA_CTRL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	CSA_BLK_LVL_2	R/W	000b	Current shunt amplifier 2 blanking time. % of tDRV. 000b = 0 %, Disabled 001b = 25 % 010b = 37.5 % 011b = 50 % 100b = 62.5 % 101b = 75 % 110b = 87.5 % 111b = 100 %

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8.4.3 DRV8714-Q1_CONTROL_ADV Registers

Table 8-109 lists the DRV8714-Q1_CONTROL_ADV registers. All register offset addresses not listed in Table 8-109 should be considered as reserved locations and the register contents should not be modified.

Table 8-109. DRV8714-Q1_CONTROL_ADV Registers

Address	Acronym	Register Name	Section
2Ah	AGD_CTRL1	Adaptive gate drive general control functions	Go
2Bh	PDR_CTRL1	Half-bridge 1 and 2 PDR delay and max current settings	Go
2Ch	PDR_CTRL2	Half-bridge 3 and 4 PDR delay and max current settings	Go
2Dh	PDR_CTRL3	Half-bridge 5 and 6 PDR delay and max current settings	Go
2Eh	PDR_CTRL4	Half-bridge 7 and 8 PDR delay and max current settings	Go
2Fh	PDR_CTRL5	Half-bridge 1 PDR charge and discharge initial settings.	Go
30h	PDR_CTRL6	Half-bridge PDR charge and discharge initial settings.	Go
31h	PDR_CTRL7	Half-bridge 3 PDR charge and discharge initial settings.	Go
32h	PDR_CTRL8	Half-bridge 4 PDR charge and discharge initial settings.	Go
33h	PDR_CTRL9	Half-bridge 1 and 2 PDR loop controller gain	Go
34h	PDR_CTRL10	Half-bridge 3 and 4 PDR loop controller gain	Go
35h	STC_CTRL1	Half-bridge 1 STC rise/fall time and controller gain	Go
36h	STC_CTRL2	Half-bridge 2 STC rise/fall time and controller gain	Go
37h	STC_CTRL3	Half-bridge 3 STC rise/fall time and controller gain	Go
38h	STC_CTRL4	Half-bridge 4 STC rise/fall time and controller gain	Go
39h	DCC_CTRL1	Half-bridge 1-4 DCC enable and manual control	Go
3Ah	PST_CTRL1	Half-bridge 1-4 freewheel and post charge delay control	Go
3Bh	PST_CTRL2	Half-bridge 1-4 post charge controller gain	Go

Complex bit access types are encoded to fit into small table cells. Table 8-110 shows the codes that are used for access types in this section.

Table 8-110. DRV8714-Q1_CONTROL_ADV Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
- *n*		Value after reset or the default value

8.4.3.1 AGD_CTRL1 Register (Address = 2Ah) [Reset = 40h]

AGD_CTRL1 is shown in Figure 8-93 and described in Table 8-111.

Return to the Summary Table.

Control register for adaptive gate drive voltage thresholds, pull down setting, and active half-bridge configuration.

Figure 8-93. AGD_CTRL1 Register

7	6	5	4	3	2	1	0
AGD_THR		AGD_ISTRONG		RESERVED			
R/W-01b		R/W-00b		R-0000b			

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Table 8-111. AGD_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	AGD_THR	R/W	01b	Adaptive gate driver VSH threshold configuration. 00b = 1V, VDRAIN - 0.5V 01b = 1V, VDRAIN - 1V 10b = 2V, VDRAIN - 1.5V 11b = 2V, VDRAIN - 2V
5-4	AGD_ISTRONG	R/W	00b	Adaptive gate driver ISTRONG configuration. 00b = ISTRONG pulldown decoded from initial IDRVP_x register setting. 01b = 62 mA 10b = 124 mA 11b = RSVD
3-0	RESERVED	R	0000b	Reserved

8.4.3.2 PDR_CTRL1 Register (Address = 2Bh) [Reset = Ah]

PDR_CTRL1 is shown in Figure 8-94 and described in Table 8-112.

Return to the Summary Table.

Control register for tON_OFF propagation delay and pre-charge/discharge max current for half-bridge 1.

Figure 8-94. PDR_CTRL1 Register

7	6	5	4	3	2	1	0
PRE_MAX_1		T_DON_DOFF_1					
R/W-00b		R/W-001010b					

Table 8-112. PDR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRE_MAX_1	R/W	00b	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 1. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA
5-0	T_DON_DOFF_1	R/W	001010b	On and off time delay for half-bridge 1. 140 ns x T_DON_DOFF_1 [3:0] Default time: 001010b (1.4 us)

8.4.3.3 PDR_CTRL2 Register (Address = 2Ch) [Reset = Ah]

PDR_CTRL2 is shown in Figure 8-95 and described in Table 8-113.

Return to the Summary Table.

Control register for tON_OFF propagation delay and pre-charge/discharge max current for half-bridge 2.

Figure 8-95. PDR_CTRL2 Register

7	6	5	4	3	2	1	0
PRE_MAX_2		T_DON_DOFF_2					
R/W-00b		R/W-001010b					

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Table 8-113. PDR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRE_MAX_2	R/W	00b	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 2. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA
5-0	T_DON_DOFF_2	R/W	001010b	On and off time delay for half-bridge 2. 140 ns x T_DON_DOFF_2 [3:0] Default time: 001010b (1.4 us)

8.4.3.4 PDR_CTRL3 Register (Address = 2Dh) [Reset = Ah]

PDR_CTRL3 is shown in Figure 8-96 and described in Table 8-114.

Return to the Summary Table.

Control register for tON_OFF propagation delay and pre-charge/discharge max current for half-bridge 3.

Figure 8-96. PDR_CTRL3 Register

7	6	5	4	3	2	1	0
PRE_MAX_3		T_DON_DOFF_3					
R/W-00b		R/W-001010b					

Table 8-114. PDR_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRE_MAX_3	R/W	00b	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 3. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA
5-0	T_DON_DOFF_3	R/W	001010b	On and off time delay for half-bridge 3. 140 ns x T_DON_DOFF_3 [3:0] Default time: 001010b (1.4 us)

8.4.3.5 PDR_CTRL4 Register (Address = 2Eh) [Reset = Ah]

PDR_CTRL4 is shown in Figure 8-97 and described in Table 8-115.

Return to the Summary Table.

Control register for tON_OFF propagation delay and pre-charge/discharge max current for half-bridge 4.

Figure 8-97. PDR_CTRL4 Register

7	6	5	4	3	2	1	0
PRE_MAX_4		T_DON_DOFF_4					
R/W-00b		R/W-001010b					

Table 8-115. PDR_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRE_MAX_4	R/W	00b	Maximum gate drive current limit for pre-charge and pre-discharge for half-bridge 4. 00b = 64 mA 01b = 32 mA 10b = 16 mA 11b = 8 mA

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Table 8-115. PDR_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	T_DON_DOFF_4	R/W	001010b	On and off time delay for half-bridge 4. 140 ns x T_DON_DOFF_4 [3:0] Default time: 001010b (1.4 us)

8.4.3.6 PDR_CTRL5 Register (Address = 2Fh) [Reset = F6h]

PDR_CTRL5 is shown in Figure 8-98 and described in Table 8-116.

Return to the Summary Table.

Control register for charge and pre-charge initial settings for half-bridge 1.

Figure 8-98. PDR_CTRL5 Register

7	6	5	4	3	2	1	0
T_PRE_CHR_1		T_PRE_DCHR_1		PRE_CHR_INIT_1		PRE_DCHR_INIT_1	
R/W-11b		R/W-11b		R/W-01b		R/W-10b	

Table 8-116. PDR_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	T_PRE_CHR_1	R/W	11b	PDR control loop pre-charge time for half-bridge 1. Set as ratio of T_DON_DOFF_1 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR_1	R/W	11b	PDR control loop pre-discharge time for half-bridge 1. Set as ratio of T_DON_DOFF_1 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT_1	R/W	01b	PDR control loop initial pre-charge current setting for half-bridge 1. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA
1-0	PRE_DCHR_INIT_1	R/W	10b	PDR control loop initial pre-discharge current setting for half-bridge 1. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.4.3.7 PDR_CTRL6 Register (Address = 30h) [Reset = F6h]

PDR_CTRL6 is shown in Figure 8-99 and described in Table 8-117.

Return to the Summary Table.

Control register for charge and pre-charge initial settings for half-bridge 2.

Figure 8-99. PDR_CTRL6 Register

7	6	5	4	3	2	1	0
T_PRE_CHR_2		T_PRE_DCHR_2		PRE_CHR_INIT_2		PRE_DCHR_INIT_2	
R/W-11b		R/W-11b		R/W-01b		R/W-10b	

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Table 8-117. PDR_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	T_PRE_CHR_2	R/W	11b	PDR control loop pre-charge time for half-bridge 2. Set as ratio of T_DON_DOFF_2 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR_2	R/W	11b	PDR control loop pre-discharge time for half-bridge 2. Set as ratio of T_DON_DOFF_2 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT_2	R/W	01b	PDR control loop initial pre-charge current setting for half-bridge 2. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA
1-0	PRE_DCHR_INIT_2	R/W	10b	PDR control loop initial pre-discharge current setting for half-bridge 2. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.4.3.8 PDR_CTRL7 Register (Address = 31h) [Reset = F6h]

PDR_CTRL7 is shown in Figure 8-100 and described in Table 8-118.

Return to the Summary Table.

Control register for charge and pre-charge initial settings for half-bridge 3.

Figure 8-100. PDR_CTRL7 Register

7	6	5	4	3	2	1	0
T_PRE_CHR_3		T_PRE_DCHR_3		PRE_CHR_INIT_3		PRE_DCHR_INIT_3	
R/W-11b		R/W-11b		R/W-01b		R/W-10b	

Table 8-118. PDR_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	T_PRE_CHR_3	R/W	11b	PDR control loop pre-charge time for half-bridge 3. Set as ratio of T_DON_DOFF_3 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR_3	R/W	11b	PDR control loop pre-discharge time for half-bridge 3. Set as ratio of T_DON_DOFF_3 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT_3	R/W	01b	PDR control loop initial pre-charge current setting for half-bridge 3. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

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Table 8-118. PDR_CTRL7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PRE_DCHR_INIT_3	R/W	10b	PDR control loop initial pre-discharge current setting for half-bridge 3. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.4.3.9 PDR_CTRL8 Register (Address = 32h) [Reset = F6h]

PDR_CTRL8 is shown in Figure 8-101 and described in Table 8-119.

Return to the Summary Table.

Control register for charge and pre-charge initial settings for half-bridge 4.

Figure 8-101. PDR_CTRL8 Register

7	6	5	4	3	2	1	0
T_PRE_CHR_4		T_PRE_DCHR_4		PRE_CHR_INIT_4		PRE_DCHR_INIT_4	
R/W-11b		R/W-11b		R/W-01b		R/W-10b	

Table 8-119. PDR_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	T_PRE_CHR_4	R/W	11b	PDR control loop pre-charge time for half-bridge 4. Set as ratio of T_DON_DOFF_4 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
5-4	T_PRE_DCHR_4	R/W	11b	PDR control loop pre-discharge time for half-bridge 4. Set as ratio of T_DON_DOFF_4 [5:0] 00b = 1/8 01b = 1/4 10b = 3/8 11b = 1/2
3-2	PRE_CHR_INIT_4	R/W	01b	PDR control loop initial pre-charge current setting for half-bridge 4. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA
1-0	PRE_DCHR_INIT_4	R/W	10b	PDR control loop initial pre-discharge current setting for half-bridge 4. 00b = 4 mA 01b = 8 mA 10b = 16 mA 11b = 32 mA

8.4.3.10 PDR_CTRL9 Register (Address = 33h) [Reset = 11h]

PDR_CTRL9 is shown in Figure 8-102 and described in Table 8-120.

Return to the Summary Table.

Control register to configure PDR Kp loop controller gain setting for half-bridges 1 and 2.

Figure 8-102. PDR_CTRL9 Register

7	6	5	4	3	2	1	0
EN_PDR_1	PDR_ERR_1	KP_PDR_1		EN_PDR_2	PDR_ERR_2	KP_PDR_2	

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Figure 8-102. PDR_CTRL9 Register (continued)

R/W-0b	R/W-0b	R/W-01b	R/W-0b	R/W-0b	R/W-01b

Table 8-120. PDR_CTRL9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_PDR_1	R/W	0b	Enable PDR loop control for half-bridge 1.
6	PDR_ERR_1	R/W	0b	PDR loop error limit for half-bridge 1. 0b = 1-bit error 1b = Actual error
5-4	KP_PDR_1	R/W	01b	PDR proportional controller gain setting for half-bridge 1. 00b = 1 01b = 2 10b = 3 11b = 4
3	EN_PDR_2	R/W	0b	Enable PDR loop control for half-bridge 2.
2	PDR_ERR_2	R/W	0b	PDR loop error limit for half-bridge 2. 0b = 1-bit error 1b = Actual error
1-0	KP_PDR_2	R/W	01b	PDR proportional controller gain setting for half-bridge 2. 00b = 1 01b = 2 10b = 3 11b = 4

8.4.3.11 PDR_CTRL10 Register (Address = 34h) [Reset = 11h]

PDR_CTRL10 is shown in Figure 8-103 and described in Table 8-121.

Return to the Summary Table.

Control register to configure PDR Kp loop controller gain setting for half-bridges 3 and 4.

Figure 8-103. PDR_CTRL10 Register

7	6	5	4	3	2	1	0
EN_PDR_3	PDR_ERR_3	KP_PDR_3		EN_PDR_4	PDR_ERR_4	KP_PDR_4	
R/W-0b	R/W-0b	R/W-01b		R/W-0b	R/W-0b	R/W-01b	

Table 8-121. PDR_CTRL10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_PDR_3	R/W	0b	Enable PDR loop control for half-bridge 3.
6	PDR_ERR_3	R/W	0b	PDR loop error limit for half-bridge 3. 0b = 1-bit error 1b = Actual error
5-4	KP_PDR_3	R/W	01b	PDR proportional controller gain setting for half-bridge 3. 00b = 1 01b = 2 10b = 3 11b = 4
3	EN_PDR_4	R/W	0b	Enable PDR loop control for half-bridge 4.
2	PDR_ERR_4	R/W	0b	PDR loop error limit for half-bridge 4. 0b = 1-bit error 1b = Actual error
1-0	KP_PDR_4	R/W	01b	PDR proportional controller gain setting for half-bridge 4. 00b = 1 01b = 2 10b = 3 11b = 4

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8.4.3.12 STC_CTRL1 Register (Address = 35h) [Reset = 23h]

STC_CTRL1 is shown in Figure 8-104 and described in Table 8-122.

Return to the Summary Table.

Control register to configure STC rise/fall time and Kp loop controller gain setting for half-bridge 1.

Figure 8-104. STC_CTRL1 Register

7	6	5	4	3	2	1	0
T_RISE_FALL_1				EN_STC_1	STC_ERR_1	KP_STC_1	
R/W-0010b				R/W-0b	R/W-0b	R/W-11b	

Table 8-122. STC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	T_RISE_FALL_1	R/W	0010b	Set switch-node VSH rise and fall time for half-bridge 1. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us
3	EN_STC_1	R/W	0b	Enable STC loop control for half-bridge 1.
2	STC_ERR_1	R/W	0b	STC loop error limit for half-bridge 1. 0b = 1-bit error 1b = Actual error
1-0	KP_STC_1	R/W	11b	STC proportional controller gain setting for half-bridge 1. 00b = 1 01b = 2 10b = 3 11b = 4

8.4.3.13 STC_CTRL2 Register (Address = 36h) [Reset = 23h]

STC_CTRL2 is shown in Figure 8-105 and described in Table 8-123.

Return to the Summary Table.

Control register to configure STC rise/fall time and Kp loop controller gain setting for half-bridge 2.

Figure 8-105. STC_CTRL2 Register

7	6	5	4	3	2	1	0
T_RISE_FALL_2				EN_STC_2	STC_ERR_2	KP_STC_2	
R/W-0010b				R/W-0b	R/W-0b	R/W-11b	

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Table 8-123. STC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	T_RISE_FALL_2	R/W	0010b	Set switch-node VSH rise and fall time for half-bridge 2. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us
3	EN_STC_2	R/W	0b	Enable STC loop control for half-bridge 2.
2	STC_ERR_2	R/W	0b	STC loop error limit for half-bridge 2. 0b = 1-bit error 1b = Actual error
1-0	KP_STC_2	R/W	11b	STC proportional controller gain setting for half-bridge 2. 00b = 1 01b = 2 10b = 3 11b = 4

8.4.3.14 STC_CTRL3 Register (Address = 37h) [Reset = 23h]

STC_CTRL3 is shown in Figure 8-106 and described in Table 8-124.

Return to the Summary Table.

Control register to configure STC rise/fall time and Kp loop controller gain setting for half-bridge 3.

Figure 8-106. STC_CTRL3 Register

7	6	5	4	3	2	1	0
T_RISE_FALL_3				EN_STC_3	STC_ERR_3	KP_STC_3	
R/W-0010b				R/W-0b	R/W-0b	R/W-11b	

Table 8-124. STC_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	T_RISE_FALL_3	R/W	0010b	Set switch-node VSH rise and fall time for half-bridge 3. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us

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Table 8-124. STC_CTRL3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	EN_STC_3	R/W	0b	Enable STC loop control for half-bridge 3.
2	STC_ERR_3	R/W	0b	STC loop error limit for half-bridge 3. 0b = 1-bit error 1b = Actual error
1-0	KP_STC_3	R/W	11b	STC proportional controller gain setting for half-bridge 3. 00b = 1 01b = 2 10b = 3 11b = 4

8.4.3.15 STC_CTRL4 Register (Address = 38h) [Reset = 23h]

STC_CTRL4 is shown in Figure 8-107 and described in Table 8-125.

Return to the Summary Table.

Control register to configure STC rise/fall time and Kp loop controller gain setting for half-bridge 4.

Figure 8-107. STC_CTRL4 Register

7	6	5	4	3	2	1	0
T_RISE_FALL_4				EN_STC_4	STC_ERR_4	KP_STC_4	
R/W-0010b				R/W-0b	R/W-0b	R/W-11b	

Table 8-125. STC_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	T_RISE_FALL_4	R/W	0010b	Set switch-node VSH rise and fall time for half-bridge 4. 0000b = 0.35 us 0001b = 0.56 us 0010b = 0.77 us 0011b = 0.98 us 0100b = 1.33 us 0101b = 1.68 us 0110b = 2.03 us 0111b = 2.45 us 1000b = 2.94 us 1001b = 3.99 us 1010b = 4.97 us 1011b = 5.95 us 1100b = 7.98 us 1101b = 9.94 us 1110b = 11.97 us 1111b = 15.96 us
3	EN_STC_4	R/W	0b	Enable STC loop control for half-bridge 4.
2	STC_ERR_4	R/W	0b	STC loop error limit for half-bridge 4. 0b = 1-bit error 1b = Actual error
1-0	KP_STC_4	R/W	11b	STC proportional controller gain setting for half-bridge 4. 00b = 1 01b = 2 10b = 3 11b = 4

8.4.3.16 DCC_CTRL1 Register (Address = 39h) [Reset = 0h]

DCC_CTRL1 is shown in Figure 8-108 and described in Table 8-126.

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Control register to enable DCC loop and manual configuration for half-bridges 1-4.

Figure 8-108. DCC_CTRL1 Register

7	6	5	4	3	2	1	0
EN_DCC_1	EN_DCC_2	EN_DCC_3	EN_DCC_4	IDIR_MAN_1	IDIR_MAN_2	IDIR_MAN_3	IDIR_MAN_4
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-126. DCC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_DCC_1	R/W	0b	Enable duty cycle compensation for half-bridge 1.
6	EN_DCC_2	R/W	0b	Enable duty cycle compensation for half-bridge 2.
5	EN_DCC_3	R/W	0b	Enable duty cycle compensation for half-bridge 3.
4	EN_DCC_4	R/W	0b	Enable duty cycle compensation for half-bridge 4.
3	IDIR_MAN_1	R/W	0b	Current polarity detection mode for half-bridge 1. 0b = Automatic 1b = Manual (Set by HBx_HL)
2	IDIR_MAN_2	R/W	0b	Current polarity detection mode for half-bridge 2. 0b = Automatic 1b = Manual (Set by HBx_HL)
1	IDIR_MAN_3	R/W	0b	Current polarity detection mode for half-bridge 3. 0b = Automatic 1b = Manual (Set by HBx_HL)
0	IDIR_MAN_4	R/W	0b	Current polarity detection mode for half-bridge 4. 0b = Automatic 1b = Manual (Set by HBx_HL)

8.4.3.17 PST_CTRL1 Register (Address = 3Ah) [Reset = Fh]

PST_CTRL1 is shown in Figure 8-109 and described in Table 8-127.

Return to the Summary Table.

Control register to configure max freewheeling current and post charge delay for half-bridges 1-4.

Figure 8-109. PST_CTRL1 Register

7	6	5	4	3	2	1	0
FW_MAX_1	FW_MAX_2	FW_MAX_3	FW_MAX_4	EN_PST_DLY_1	EN_PST_DLY_2	EN_PST_DLY_3	EN_PST_DLY_4
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 8-127. PST_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FW_MAX_1	R/W	0b	Gate drive current used for freewheeling MOSFET for half-bridge 1. 0b = PRE_CHR_MAX_1 [1:0] 1b = 64 mA
6	FW_MAX_2	R/W	0b	Gate drive current used for freewheeling MOSFET for half-bridge 2. 0b = PRE_CHR_MAX_2 [1:0] 1b = 64 mA
5	FW_MAX_3	R/W	0b	Gate drive current used for freewheeling MOSFET for half-bridge 3. 0b = PRE_CHR_MAX_3 [1:0] 1b = 64 mA
4	FW_MAX_4	R/W	0b	Gate drive current used for freewheeling MOSFET for half-bridge 4. 0b = PRE_CHR_MAX_4 [1:0] 1b = 64 mA
3	EN_PST_DLY_1	R/W	1b	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_1 - T_PRE_CHR_1.
2	EN_PST_DLY_2	R/W	1b	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_2 - T_PRE_CHR_2.

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Table 8-127. PST_CTRL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EN_PST_DLY_3	R/W	1b	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_3 - T_PRE_CHR_3.
0	EN_PST_DLY_4	R/W	1b	Enable post-charge time delay. Time delay is equal to T_DON_DOFF_4 - T_PRE_CHR_4.

8.4.3.18 PST_CTRL2 Register (Address = 3Bh) [Reset = 55h]

PST_CTRL2 is shown in Figure 8-110 and described in Table 8-128.

Return to the Summary Table.

Control register to configure post charge Kp loop controller gain setting for half-bridges 1-4.

Figure 8-110. PST_CTRL2 Register

7	6	5	4	3	2	1	0
KP_PST_1		KP_PST_2		KP_PST_3		KP_PST_4	
R/W-01b		R/W-01b		R/W-01b		R/W-01b	

Table 8-128. PST_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	KP_PST_1	R/W	01b	Post charge proportional control gain setting for half-bridge 1. 00b = Disabled 01b = 2 10b = 4 11b = 15
5-4	KP_PST_2	R/W	01b	Post charge proportional control gain setting for half-bridge 2. 00b = Disabled 01b = 2 10b = 4 11b = 15
3-2	KP_PST_3	R/W	01b	Post charge proportional control gain setting for half-bridge 3. 00b = Disabled 01b = 2 10b = 4 11b = 15
1-0	KP_PST_4	R/W	01b	Post charge proportional control gain setting for half-bridge 4. 00b = Disabled 01b = 2 10b = 4 11b = 15

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8.4.4 DRV8714-Q1_STATUS_ADV Registers

Table 8-129 lists the DRV8714-Q1_STATUS_ADV registers. All register offset addresses not listed in Table 8-129 should be considered as reserved locations and the register contents should not be modified.

Table 8-129. DRV8714-Q1_STATUS_ADV Registers

Address	Acronym	Register Name	Section
3Ch	SGD_STAT1	Half-bridge 1-4 current polarity indicators	Go
3Dh	SGD_STAT2	Half-bridge 1-4 PDR underflow and overflow indictors	Go
3Eh	SGD_STAT3	Half-bridge 1-4 STC fault indicator	Go

Complex bit access types are encoded to fit into small table cells. Table 8-130 shows the codes that are used for access types in this section.

Table 8-130. DRV8714-Q1_STATUS_ADV Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
- *n*		Value after reset or the default value

8.4.4.1 SGD_STAT1 Register (Address = 3Ch) [Reset = 0h]

SGD_STAT1 is shown in Figure 8-111 and described in Table 8-131.

Return to the Summary Table.

Status registers indicating current polarity for half-bridges 1-4.

Figure 8-111. SGD_STAT1 Register

7	6	5	4	3	2	1	0
IDIR_1	IDIR_2	IDIR_3	IDIR_4	IDIR_WARN_1	IDIR_WARN_2	IDIR_WARN_3	IDIR_WARN_4
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-131. SGD_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IDIR_1	R	0b	Indicated current direction for half-bridge 1.
6	IDIR_2	R	0b	Indicated current direction for half-bridge 2.
5	IDIR_3	R	0b	Indicated current direction for half-bridge 3.
4	IDIR_4	R	0b	Indicated current direction for half-bridge 4.
3	IDIR_WARN_1	R	0b	Indicates unknown current direction for half-bridge 1.
2	IDIR_WARN_2	R	0b	Indicates unknown current direction for half-bridge 2.
1	IDIR_WARN_3	R	0b	Indicates unknown current direction for half-bridge 3.
0	IDIR_WARN_4	R	0b	Indicates unknown current direction for half-bridge 4.

8.4.4.2 SGD_STAT2 Register (Address = 3Dh) [Reset = 0h]

SGD_STAT2 is shown in Figure 8-112 and described in Table 8-132.

Return to the Summary Table.

Status registers indicating underflow and overflow in PDR loop control for half-bridges 1-4.

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Figure 8-112. SGD_STAT2 Register

7	6	5	4	3	2	1	0
PCHR_WARN_1	PCHR_WARN_2	PCHR_WARN_3	PCHR_WARN_4	PDCHR_WARN_1	PDCHR_WARN_2	PDCHR_WARN_3	PDCHR_WARN_4
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-132. SGD_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PCHR_WARN_1	R	0b	Indicates pre-charge underflow or overflow fault for half-bridge 1.
6	PCHR_WARN_2	R	0b	Indicates pre-charge underflow or overflow fault for half-bridge 2.
5	PCHR_WARN_3	R	0b	Indicates pre-charge underflow or overflow fault for half-bridge 3.
4	PCHR_WARN_4	R	0b	Indicates pre-charge underflow or overflow fault for half-bridge 4.
3	PDCHR_WARN_1	R	0b	Indicates pre-discharge underflow or overflow fault for half-bridge 1.
2	PDCHR_WARN_2	R	0b	Indicates pre-discharge underflow or overflow fault for half-bridge 2.
1	PDCHR_WARN_3	R	0b	Indicates pre-discharge underflow or overflow fault for half-bridge 3.
0	PDCHR_WARN_4	R	0b	Indicates pre-discharge underflow or overflow fault for half-bridge 4.

8.4.4.3 SGD_STAT3 Register (Address = 3Eh) [Reset = 0h]

SGD_STAT3 is shown in Figure 8-113 and described in Table 8-133.

Return to the Summary Table.

Status register indicator STC rise and fall time overflow for half-bridges 1-4.

Figure 8-113. SGD_STAT3 Register

7	6	5	4	3	2	1	0
STC_WARN_F_1	STC_WARN_F_2	STC_WARN_F_3	STC_WARN_F_4	STC_WARN_R_1	STC_WARN_R_2	STC_WARN_R_3	STC_WARN_R_4
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-133. SGD_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STC_WARN_F_1	R	0b	Indicates falling slew time TDRV overflow for half-bridge 1.
6	STC_WARN_F_2	R	0b	Indicates falling slew time TDRV overflow for half-bridge 2.
5	STC_WARN_F_3	R	0b	Indicates falling slew time TDRV overflow for half-bridge 3.
4	STC_WARN_F_4	R	0b	Indicates falling slew time TDRV overflow for half-bridge 4.
3	STC_WARN_R_1	R	0b	Indicates rising slew time TDRV overflow for half-bridge 1.
2	STC_WARN_R_2	R	0b	Indicates rising slew time TDRV overflow for half-bridge 2.
1	STC_WARN_R_3	R	0b	Indicates rising slew time TDRV overflow for half-bridge 3.
0	STC_WARN_R_4	R	0b	Indicates rising slew time TDRV overflow for half-bridge 4.

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9 Application Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DRV871x-Q1 is a highly configurable mult-channel half-bridge MOSFET gate driver than can be used to drive a variety of different output loads. The design examples below highlight how to use and configure the device for different application use cases.

9.2 Typical Application

The typical application for the DRV8718-Q1 is to control an multiple external MOSFET half-bridges for driving multiple uni-directional or bi-directional brushed DC motors. A high-level schematic example is shown below.

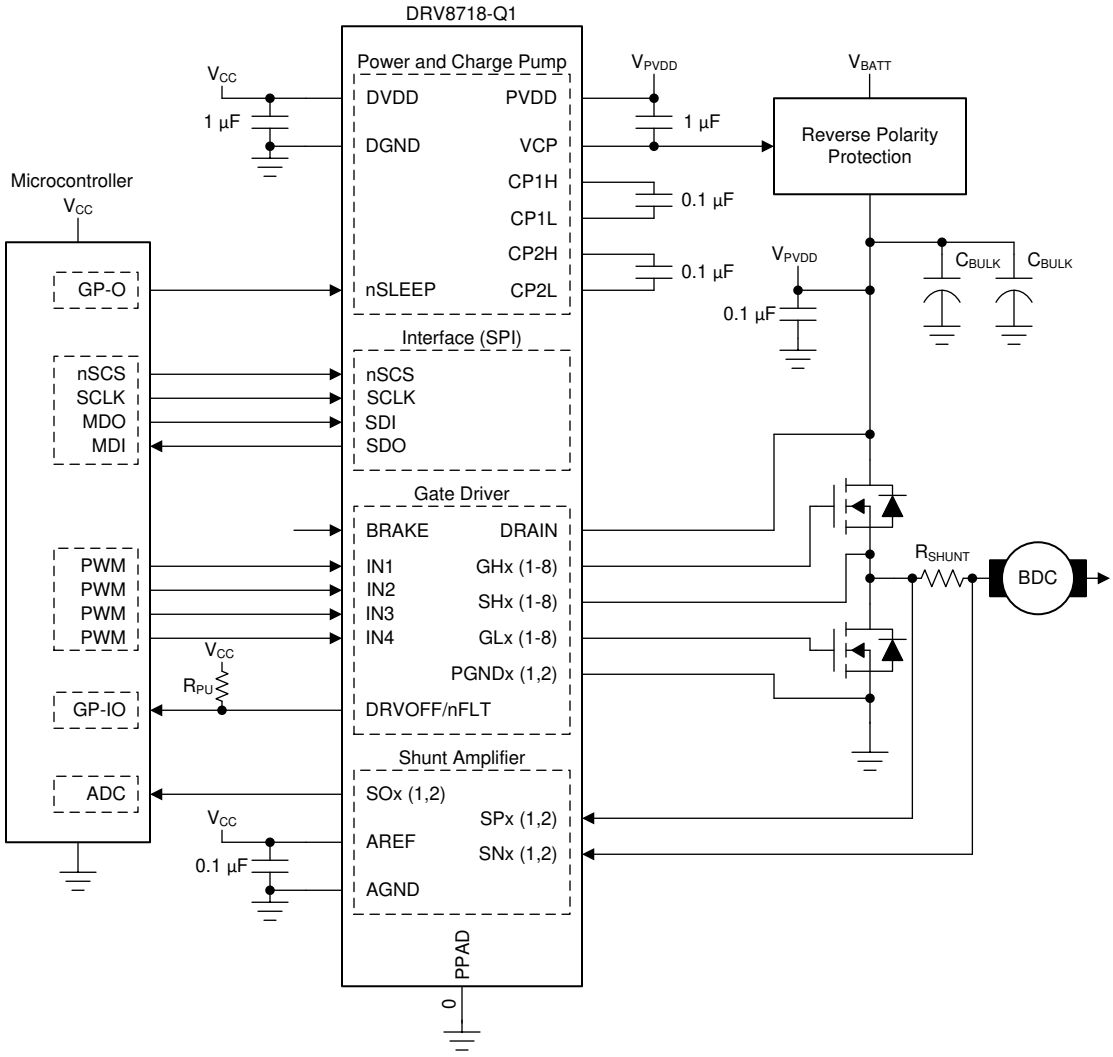

Figure 9-1. DRV8718-Q1 Typical Application

9.2.1 Design Requirements

Table 9-1 lists a set of example input parameters for the system design.

Table 9-1. Example Design Parameters

Design Parameter	Reference	Value
PVDD Nominal Supply Voltage	V_{PVDD}	12 V
PVDD Supply Voltage Range		9 to 18 V
DVDD / AREF Logic Supply Voltage	V_{CC}	3.3V
MOSFET Total Gate Charge	Q_G	30 nC (typical) at V_{GS} = 10 V
MOSFET Gate to Drain Charge	Q_{GD}	5 nC (typical)
MOSFET On Resistance	$R_{DS(on)}$	4 mΩ
Target Output Rise Time	t_{rise}	750 - 1000 ns
Target Output Fall Time	t_{fall}	250 - 500 ns
PWM Frequency	f_{PWM}	20 kHz
Maximum Motor Current	I_{MAX}	25 A
Shunt Resistor Power Capability	P_{SHUNT}	3 W

9.2.2 Detailed Design Procedure

9.2.2.1 Gate Driver Configuration

9.2.2.1.1 VCP Load Calculation Example

It should be ensured that the charge pump load capability is sufficient for the type of external MOSFET, number of PWM half-bridges, and desired PWM frequency. This can be confirmed with a simple calculation as shown in Equation 1. Since the charge pump supplies both the high-side and low-side gate drivers, the number of both switching high-side and low-side MOSFETs should be taken into consideration. This will depend on both the number of PWM half-bridges and the freewheeling mode (if the opposite MOSFET is being switched).

$$I_{VCP}\ (A) = Q_G\ (C) \times f_{PWM}\ (Hz) \times \#\ \text{of switching FETs} \quad (1)$$

Using the input design parameters as an example, we can show that in this scenario that output load capability of the charge pump is sufficient in Equation 2. For this example, four active half-bridges were assumed with active freewheeling totaling 8 switching MOSFETs.

$$I_{VCP} = 30\ nC \times 20\ kHz \times 8 = 4.8\ mA \quad (2)$$

9.2.2.1.2 I_{DRIVE} Calculation Example

The gate drive current strength, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the switch-node. If I_{DRIVE} is selected to be too low for a given MOSFET, then the MOSFET may not turn on or off completely within the configured t_{DRIVE} time and a gate fault may be asserted. Additionally, slow rise and fall times will lead to higher switching power losses in the external power MOSFETs. It is recommended to verify these values in system with the required external MOSFETs and load to determine the optimal settings.

The I_{DRIVEP} and I_{DRIVEN} for both the high-side and low-side external MOSFETs are adjustable on SPI device variants. On hardware interface device variants, both source and sink settings are selected simultaneously on the IDRIVE pin.

For MOSFETs with a known gate-to-drain charge (Q_{GD}), desired rise time (t_{rise}), and a desired fall time (t_{fall}), use Equation 3 and Equation 4 to calculate the approximate values of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} = Q_{GD} / t_{rise} \quad (3)$$

$$I_{DRIVEN} = Q_{GD} / t_{fall} \quad (4)$$

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Using the input design parameters as an example, we can calculate the approximate values for I_{DRIVEP} and I_{DRIVEN}.

$$I_{DRIVEP_HI} = 5\ nC / 750\ ns = 6.67\ mA \quad (5)$$

$$I_{DRIVEP_LO} = 5\ nC / 1000\ ns = 5\ mA \quad (6)$$

Based on these calculations a value of 6 mA was chosen for I_{DRIVEP}.

$$I_{DRIVEN_HI} = 5\ nC / 250\ ns = 20\ mA \quad (7)$$

$$I_{DRIVEN_LO} = 5\ nC / 500\ ns = 10\ mA \quad (8)$$

Based on these calculations, a value of 16 mA was chosen for I_{DRIVEN}.

9.2.2.1.3 t_{DRIVE} Calculation Example

The driver gate to source monitor timeout (t_{DRIVE}) should be configured to allow sufficient time for the external MOSFETs to charge and discharge for the selected I_{DRIVE} gate current. By default, the setting is 8us which is sufficient for many systems. The determine an appropriate t_{DRIVE} value, Equation 9 can be utilized.

$$t_{DRIVE} > Q_{G_TOT} / I_{DRIVE} \quad (9)$$

Using the input design parameters as an example, we can calculate the approximate values for t_{DRIVE}.

$$t_{DRIVE} > 30\ nC / 6\ mA = 5\ us \quad (10)$$

Based on these calculations a value of 8 us was chosen for t_{DRIVE}.

9.2.2.1.4 Maximum PWM Switching Frequency

The maximum PWM frequency of the driver is typically determined by multiple factors in the system. While the DRV871x-Q1 device can support up to 100kHz, system parameters may limit this to a lower value.

These system parameters include:

- The rise and fall times of the external MOSFETs.
- The MOSFET Q_G and load on the charge pump.
- The minimum and maximum duty cycle requirements (Ex. 10% to 90%)

9.2.2.2 Current Shunt Amplifier Configuration

The DRV871x-Q1 differential shunt amplifier gain and shunt resistor value are selected based on the dynamic current range, reference voltage supply, shunt resistor power rating, and operating temperature range. In bidirectional operation of the shunt amplifier, the dynamic range at the output is approximately calculated as shown in Equation 11. The output of the amplifier can swing from the midpoint reference (V_{AREF} / 2) to either 0.25 V or V_{AREF} - 0.25V depending on the polarity of the input voltage to the amplifier.

$$V_{SO_BI} = (V_{AREF} - 0.25\ V) - (V_{AREF} / 2) \quad (11)$$

If only unidirectional current sensing is required, the amplifier reference can be modified to expand the dynamic range at the output. The is modified through the CSA_DIV SPI register setting. In this mode, the dynamic range at the output is approximately calculated as shown in Equation 12.

$$V_{SO_UNI} = (V_{AREF} - 0.25\ V) - (V_{AREF} / 8) \quad (12)$$

Based on V_{AREF} = 3.3 V, the dynamic out range in both bidirectional or unidirectional sensing can be calculated as shown below:

$$V_{SO_BI} = (3.3\ V - 0.25\ V) - (3.3\ V / 2) = 1.4\ V \quad (13)$$

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$$V_{SO_UNI} = (3.3\ V - 0.25\ V) - (3.3\ V / 8) = 2.6375\ V \quad (14)$$

The external shunt resistor value and shunt amplifier gain setting are selected based on the available dynamic output range, the shunt resistor power rating, and maximum motor current that needs to be measured. This exact values for the shunt resistance and amplifier gain are determine by both Equation 15 and Equation 16.

$$R_{SHUNT} < P_{SHUNT} / I_{MAX}^{2} \quad (15)$$

$$A_V < V_{SO} / (I_{MAX} \times R_{SHUNT}) \quad (16)$$

Based on V_{SO} = 1.4 V, I_{MAX} = 25 A and P_{SHUNT} = 3 W, the values for shunt resistance and amplifier gain can be calculated as shown below:

$$R_{SHUNT} < 3\ W / 25^{2}\ A = 4.8\ m\Omega \quad (17)$$

$$A_V < 1.4\ V / (25\ A \times 4.8\ m\Omega) = 11.67\ V/V \quad (18)$$

Based on the results, a shunt resistance of 4 mΩ and an amplifier gain of 10 V/V can be selected.

9.2.2.3 Power Dissipation

In high ambient operating environments, it may be important to estimate the internal self heating of the driver. To determine the temperature of the device, first the internal power dissipation must be calculate. After this an estimate can be made with the device package thermal properties.

The internal power dissipation has four primary components.

- High-Side Driver Power Dissipation (P_{HS})
- Low-Side Driver Power Dissipation (P_{LS})
- PVDD Battery Supply Power Dissipation (P_{PVDD})
- DVDD/AREF Logic/Reference Supply Power Dissipation (P_{VCC})

The values for P_{HS} and P_{LS} can be approximated by referencing the earlier equation for charge pump load current as shown below. In a typical switch scenario, 4 high-side and 4 low-side MOSFET are switching.

$$I_{HS/LS}\ (A) = Q_G\ (C) \times f_{PWM}\ (Hz) \times \#\ of\ switching\ FETs \quad (19)$$

Using the input design parameters as an example, we can calculate the current load from the high-side and low-side drivers.

$$I_{HS} = 30\ nC \times 20\ kHz \times 4 = 2.4\ mA \quad (20)$$

$$I_{LS} = 30\ nC \times 20\ kHz \times 4 = 2.4\ mA \quad (21)$$

From this, the power dissipation can be calculated from the equations below for the driver power dissipation. The high-side and low-side includes a doubling factor to account for the losses in the charge pump supplying the drivers.

$$P_{HS}\ (W) = I_{HS}\ (A) \times V_{PVDD} \times 2 \quad (22)$$

$$P_{LS}\ (W) = I_{LS}\ (A) \times V_{PVDD} \times 2 \quad (23)$$

Using the input design parameters as an example, we can calculate the power dissipation from the high-side and low-side drivers.

$$P_{HS}\ (W) = 0.0576\ W = 2.4\ mA \times 12\ V \times 2 \quad (24)$$

$$P_{LS}\ (W) = 0.0576\ W = 2.4\ mA \times 12\ V \times 2 \quad (25)$$

The values for P_{PVDD} and P_{VCC} can be approximated by referencing Equation 26 and Equation 27:

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$$P_{PVDD}\ (W) = I_{PVDD}\ (A) \times V_{PVDD} \quad (26)$$

$$P_{VCC}\ (W) = (I_{DVDD}\ (A) \times V_{DVDD}) + (I_{AREF}\ (A) \times V_{AREF}) \quad (27)$$

Using the input design parameters as an example, we can calculate the power dissipation for the power supplies.

$$P_{PVDD}\ (W) = 0.162\ W = 13.5\ mA \times 12\ V \quad (28)$$

$$P_{VCC}\ (W) = 0.033\ W = (8\ mA \times 3.3\ V) + (2\ mA \times 3.3\ V) \quad (29)$$

Finally, use Equation 30 to estimate device junction temperature.

$$T_{JUNCTION}\ (°C) = T_{AMBIENT}\ (°C) + (R_{\theta JA}\ (°C/W) \times P_{TOT}(W)) \quad (30)$$

Using the previously calculated power dissipation values and the device thermal parameter from the Thermal Information table can estimate the device internal temperature:

$$T_{JUNCTION}\ (°C) = 112.9\ °C = 105\ °C + (25.6\ °C/W \times 0.3102\ W) \quad (31)$$

9.2.3 Application Curves

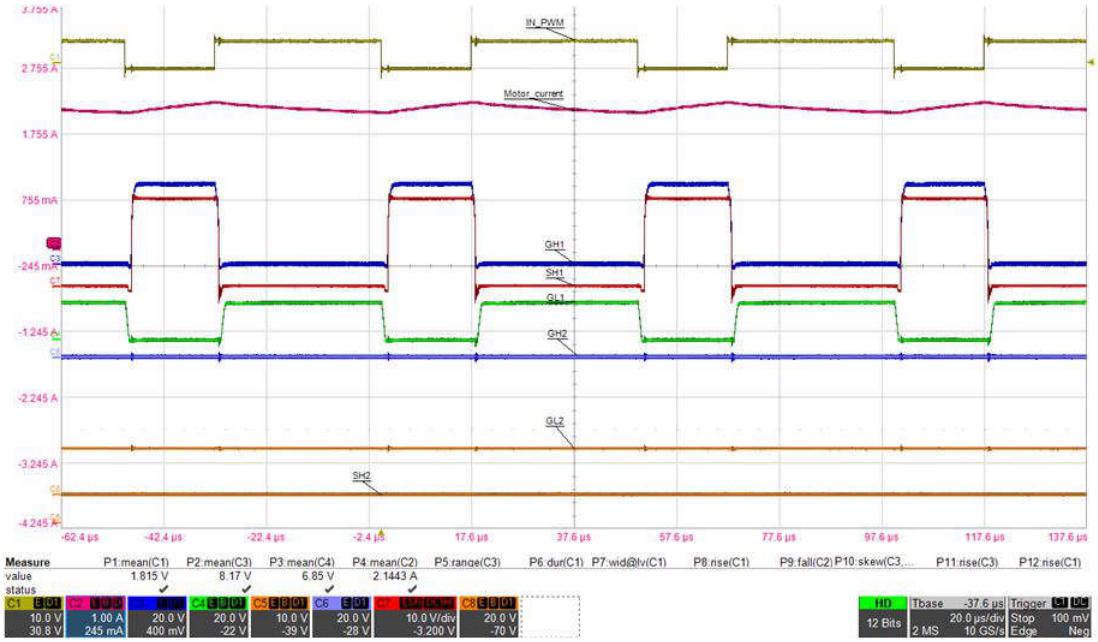

Figure 9-2. Driver Nominal PWM Operation

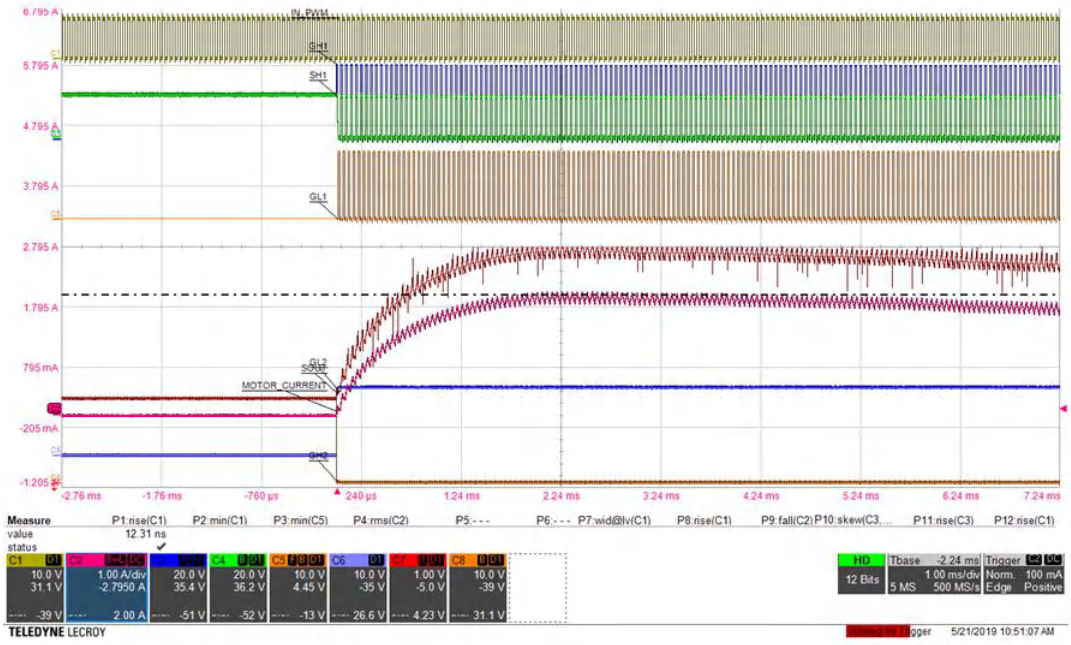

Figure 9-3. Driver Operation During Motor Startup

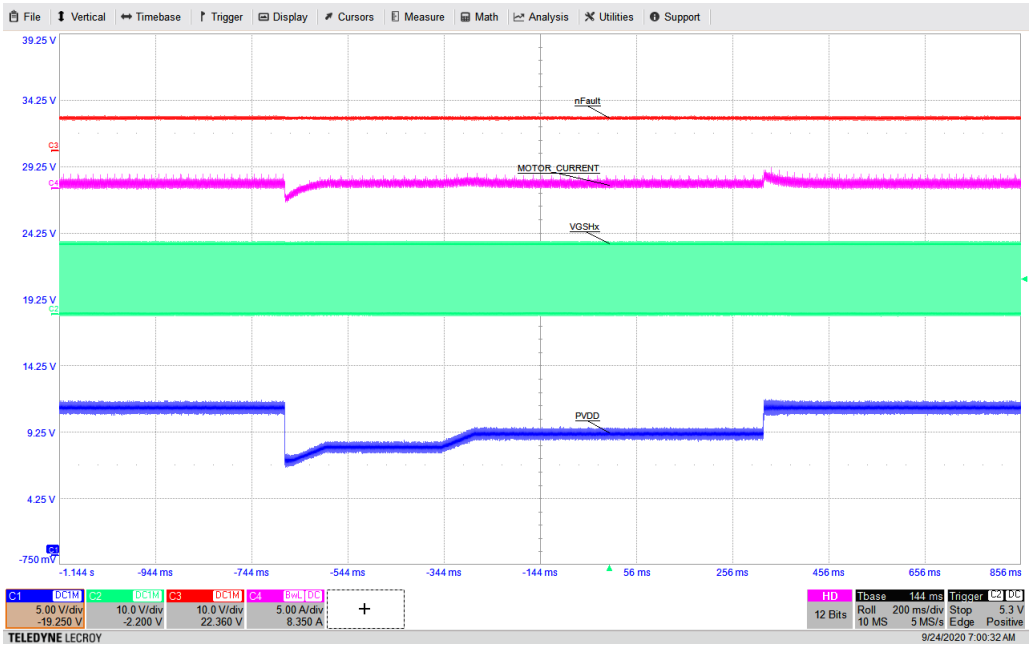

Figure 9-4. Driver PWM Operation During Warm Crank Pulse

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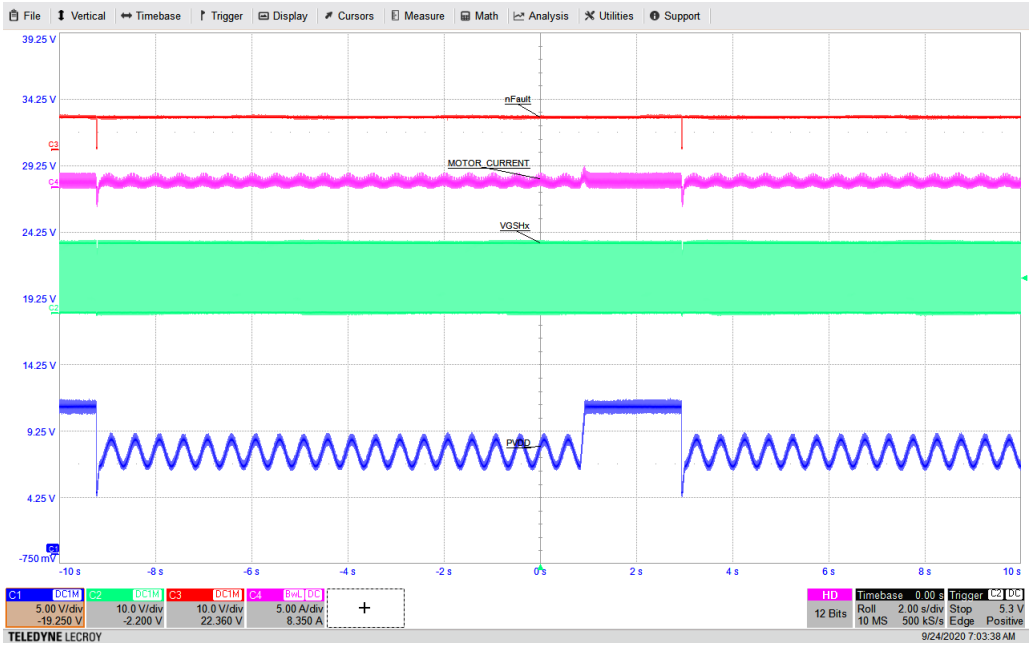

Figure 9-5. Driver PWM Operation During Cold Crank Pulse

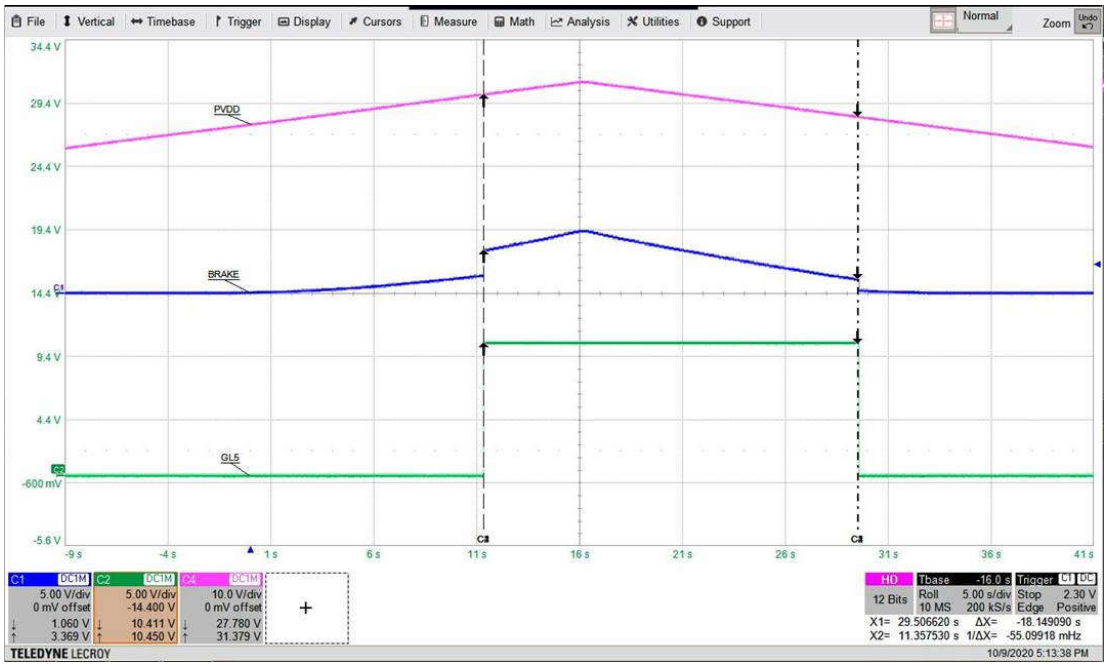

Figure 9-6. Power Off Braking Low-Side Driver Response

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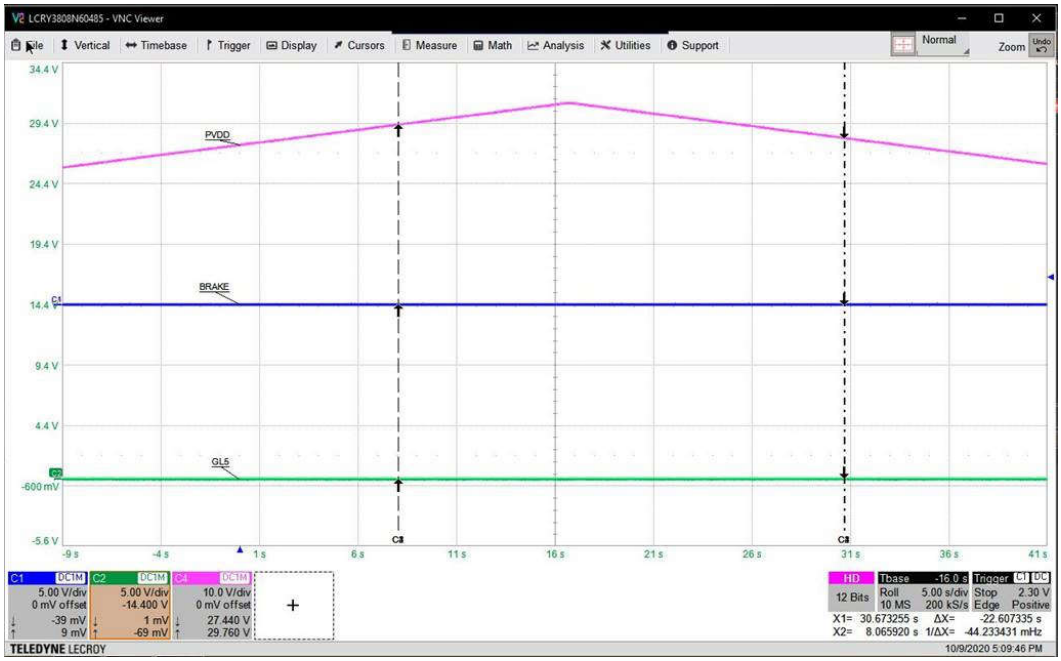

Figure 9-7. Power Off Braking Disabled

9.3 Initialization

This section provides some guidance for getting started with the DRV871x-Q1 for typical system operation.

- By default, the device is in a low-powered sleep mode with the nSLEEP pin low. In this mode, all drivers are disabled and no device communication is possible. The nSLEEP pin should be driven high, to enter its standby state.
- In the standby state, H/W interface device variants will immediately enter the active state allowing for driver operation (device settings will be derived from the pin configurations), but SPI interface device variants will power up with the drivers still disabled.
- On SPI variants, the drivers are enabled through the EN_DRV register bit. But before enabling drivers, it is recommended to configure the output drivers, sense amplifiers, setup protection circuits, and run offline diagnostics.
- The half-bridge driver PWM configurations are set through the BRG_CTRL1,2 and PWM_CTRL1,2 register and will be dependent on the output load configuration. Additionally the driver gate current level and gate driver configurations can be set through the IDRV_CTRLx and DRV_CTRLx registers.
- The sense amplifiers are configured through the CSA_CTRL1, 2, and 3 registers.
- The various protection functions can be configured through the VDS_CTRLx and UVOV_CTRL registers.
- Lastly, before enabling the drivers, offline diagnostics can be performed for open load and short circuit through the EN_OLSC and the OLSC_CTRL1,2 registers.

9.4 Power Supply Recommendations

9.4.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)

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- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

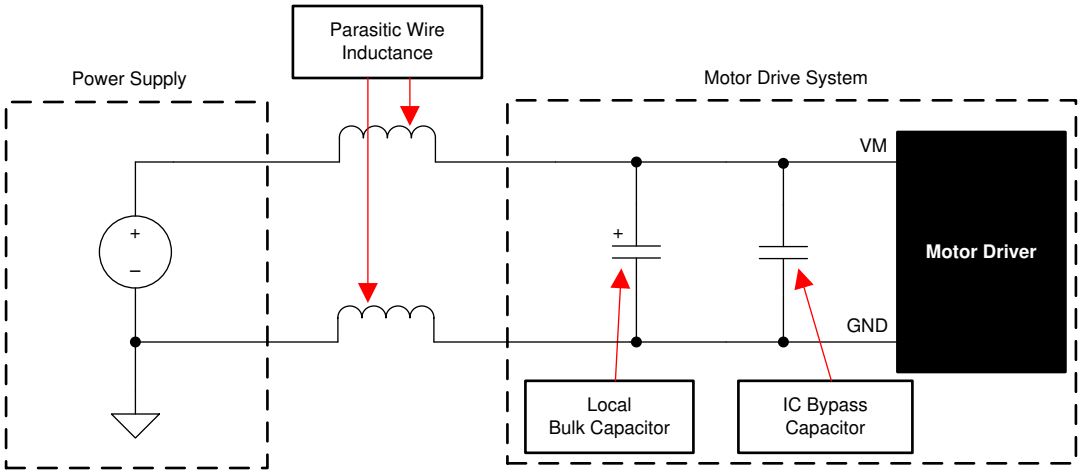

Figure 9-8. Motor Drive Supply Parasitics Example

9.5 Layout

9.5.1 Layout Guidelines

Bypass the PVDD pin to the GND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF. Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to the GND pin. Additionally, bypass the PVDD pin using a bulk capacitor rated for PVDD. This component can be electrolytic. This capacitance must be at least 10 µF. It is acceptable if this capacitance is shared with the bulk capacitance for the external power MOSFETs.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low-ESR ceramic capacitor between the CPL1 / CPH1 and CPL2 / CP2H pins. The CP1 capacitor should be 0.1 µF, rated for PVDD, and be of type X5R or X7R. The CP2 capacitor should be 0.1 µF, rated for PVDD + 16 V, and be of type X5R or X7R. Additionally, place a low-ESR ceramic capacitor between the VCP and PVDD pins. This capacitor should be 1 µF, rated for 16 V, and be of type X5R or X7R.

Bypass the DVDD pin to the DGND pin with a 1.0 µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the DGND pin. Bypass the AREF pin to the AGND pin with a 0.1 µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin. If local bypass capacitors are already present on these power supplies in close proximity of the device to minimize noise, these additional components for DVDD and/or AREF are not required.

The DRAIN pin can be shorted directly to the PVDD pin. However, if a significant distance is between the device and the external MOSFETs, use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. Ensure the PGNDx pins have a low impedance path to the sources of the low-side external

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MOSFETs and to the PCB GND plane.. pins directly to the GND plane. These recommendations allow for more accurate VDS sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGNDx pin.

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9.5.2 Layout Example

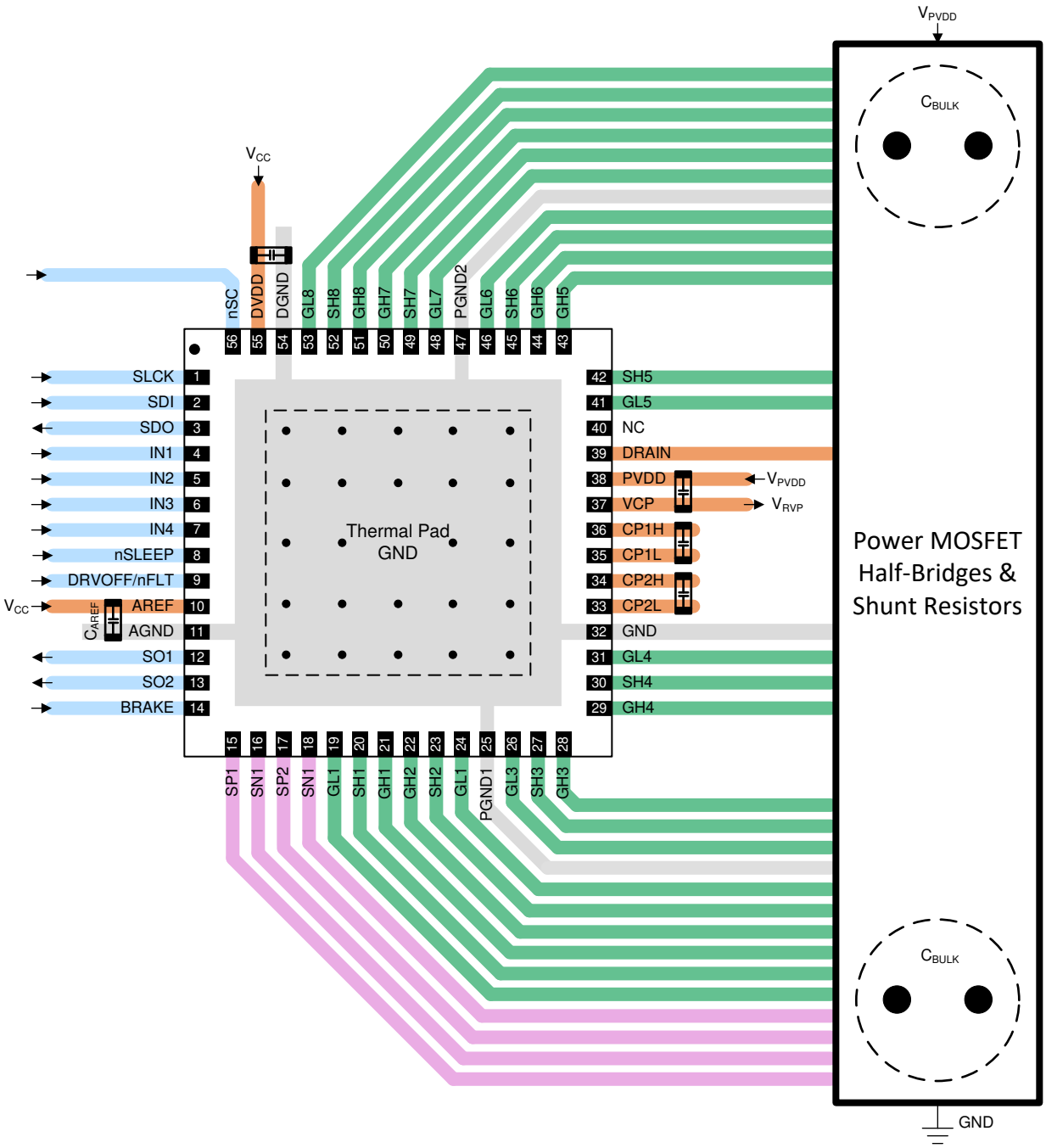

Figure 9-9. Layout Example

10 Device Documentation and Support

10.1 Documentation Support

10.1.1 Related Documents

For related documentation see the following:

- Texas Instruments, *Understanding Smart Gate Drive* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2022) to Revision D (December 2022)	Page
• Added the DRV8714A-Q1 variant	3

Changes from Revision B (June 2021) to Revision C (August 2022)	Page
• Added the QFP package option information	1

Changes from Revision A (December 2020) to Revision B (June 2021)	Page
• V_{OFF} specification improved to +/- 1mV	13

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- Amplifier CMRR MIN specification added..... 13
- Removed typo reference to ADDR_FLT.....57

Changes from Revision * (August 2020) to Revision A (December 2020)	Page
• Changed the data sheet status from Advanced Information to Production Mixed.....1	

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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12.1 Package Option Addendum

Packaging Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
DRV8714SAQRHARQ1	PREVIEW	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260 C-168 HR	-40 to 125	DRV8714S

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8714HQPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8714H
DRV8714HQPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8714H
DRV8714HQRHARQ1	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8714H
DRV8714HQRHARQ1.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8714H
DRV8714SQPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8714S
DRV8714SQPHPRQ1.A	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8714S
DRV8714SQRHARQ1	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8714S
DRV8714SQRHARQ1.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8714S
DRV8714SQRVJRQ1	Active	Production	VQFN (RVJ) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8714S
DRV8714SQRVJRQ1.A	Active	Production	VQFN (RVJ) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8714S
DRV8718SQRVJRQ1	Active	Production	VQFN (RVJ) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8718S
DRV8718SQRVJRQ1.A	Active	Production	VQFN (RVJ) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8718S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

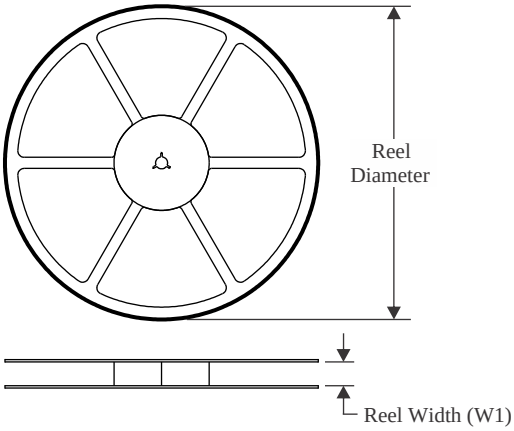
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

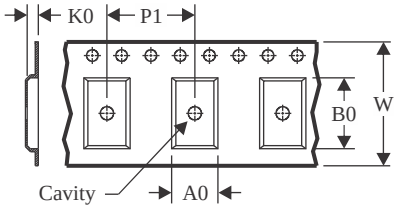
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

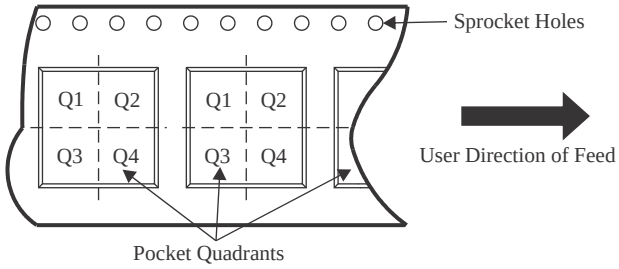


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

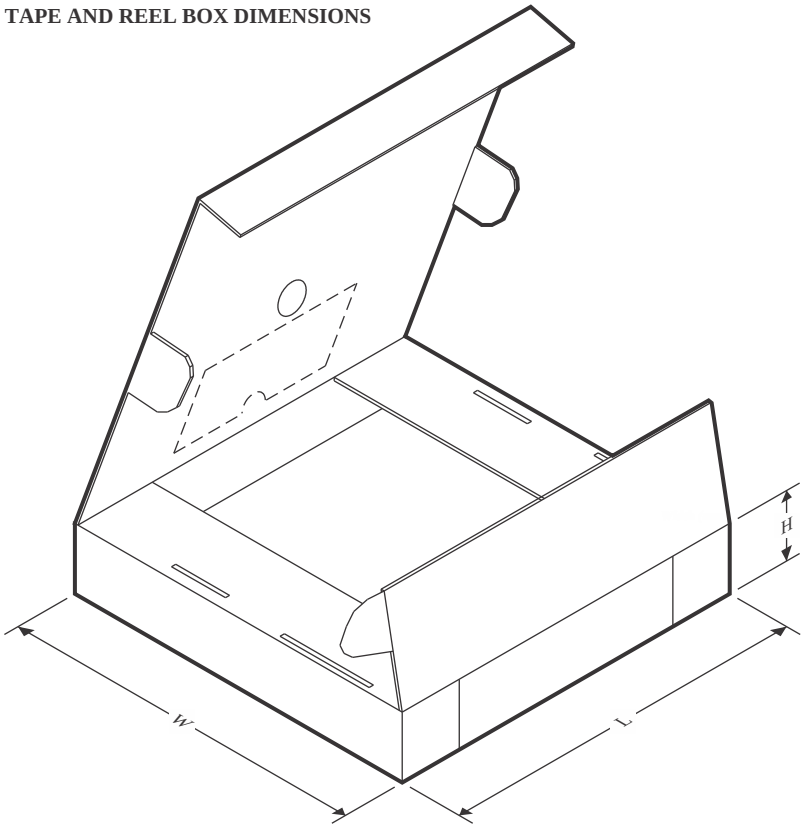
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8714HQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV8714HQRHARQ1	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8714SQPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
DRV8714SQRHARQ1	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8714SQRVJRQ1	VQFN	RVJ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
DRV8718SQRVJRQ1	VQFN	RVJ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8714HQPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8
DRV8714HQRHARQ1	VQFN	RHA	40	2500	367.0	367.0	35.0
DRV8714SQPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8
DRV8714SQRHARQ1	VQFN	RHA	40	2500	367.0	367.0	35.0
DRV8714SQRVJRQ1	VQFN	RVJ	56	2000	367.0	367.0	35.0
DRV8718SQRVJRQ1	VQFN	RVJ	56	2000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

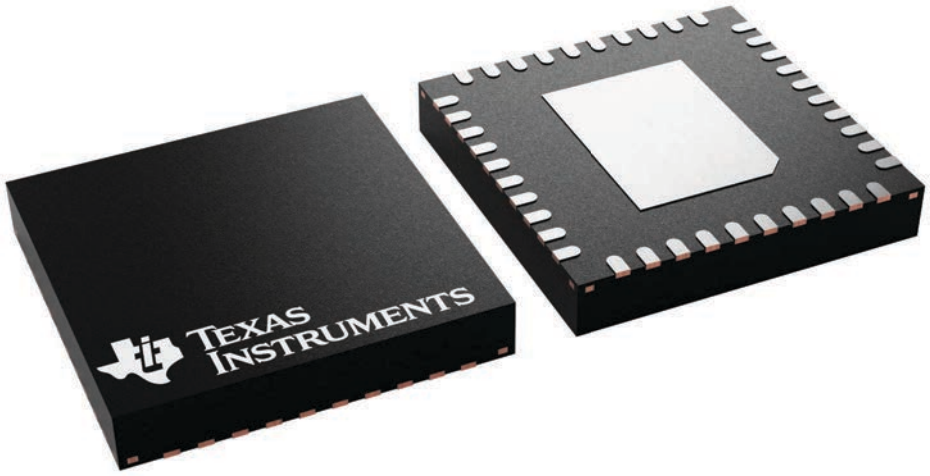
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



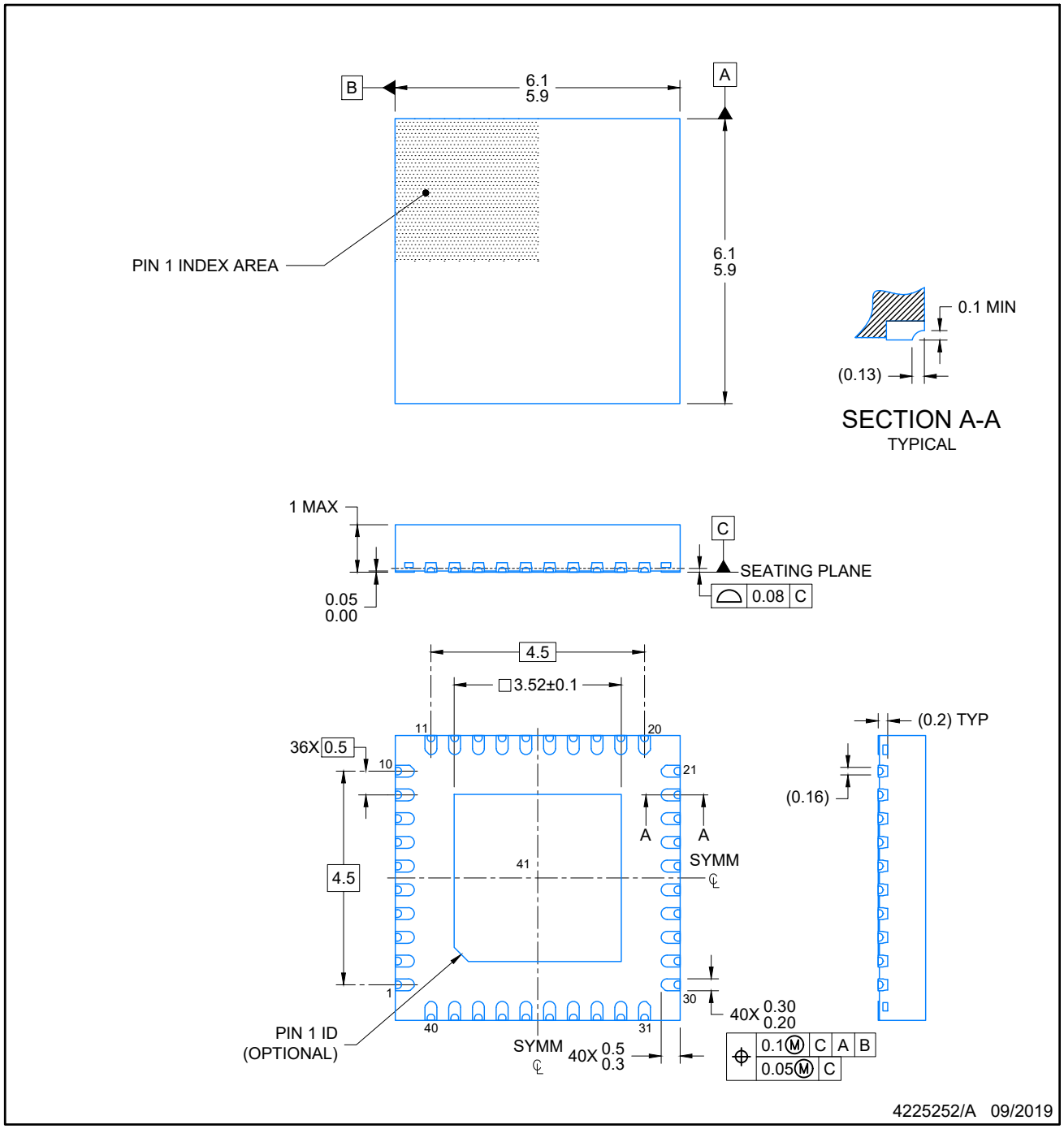
4225870/A

PACKAGE OUTLINE

RHA0040L

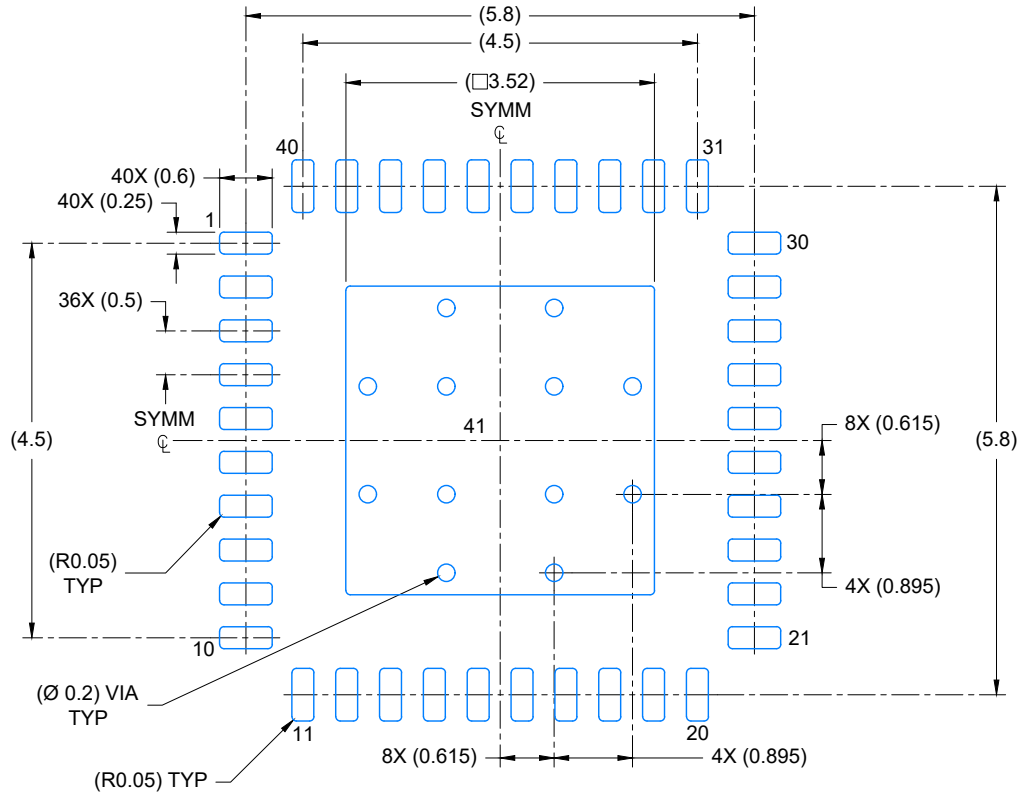
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

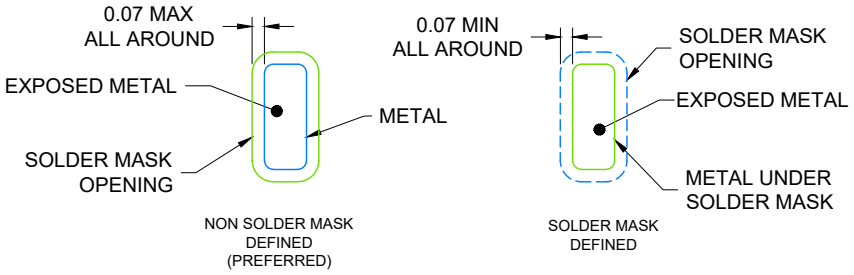


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

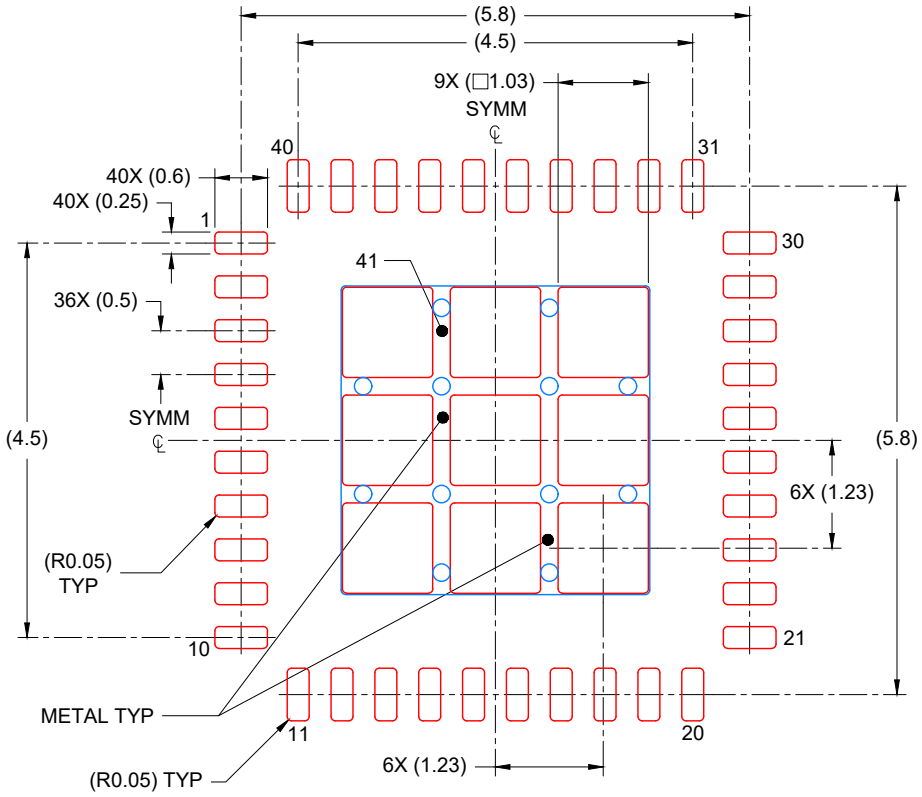


SOLDER MASK DETAILS

4225252/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
74% PRINTED COVERAGE BY AREA
SCALE: 12X

4225252/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

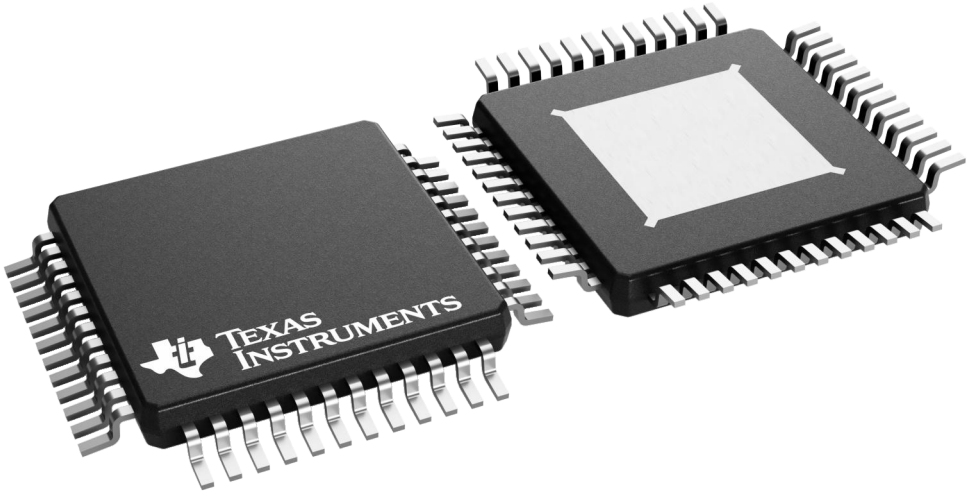
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

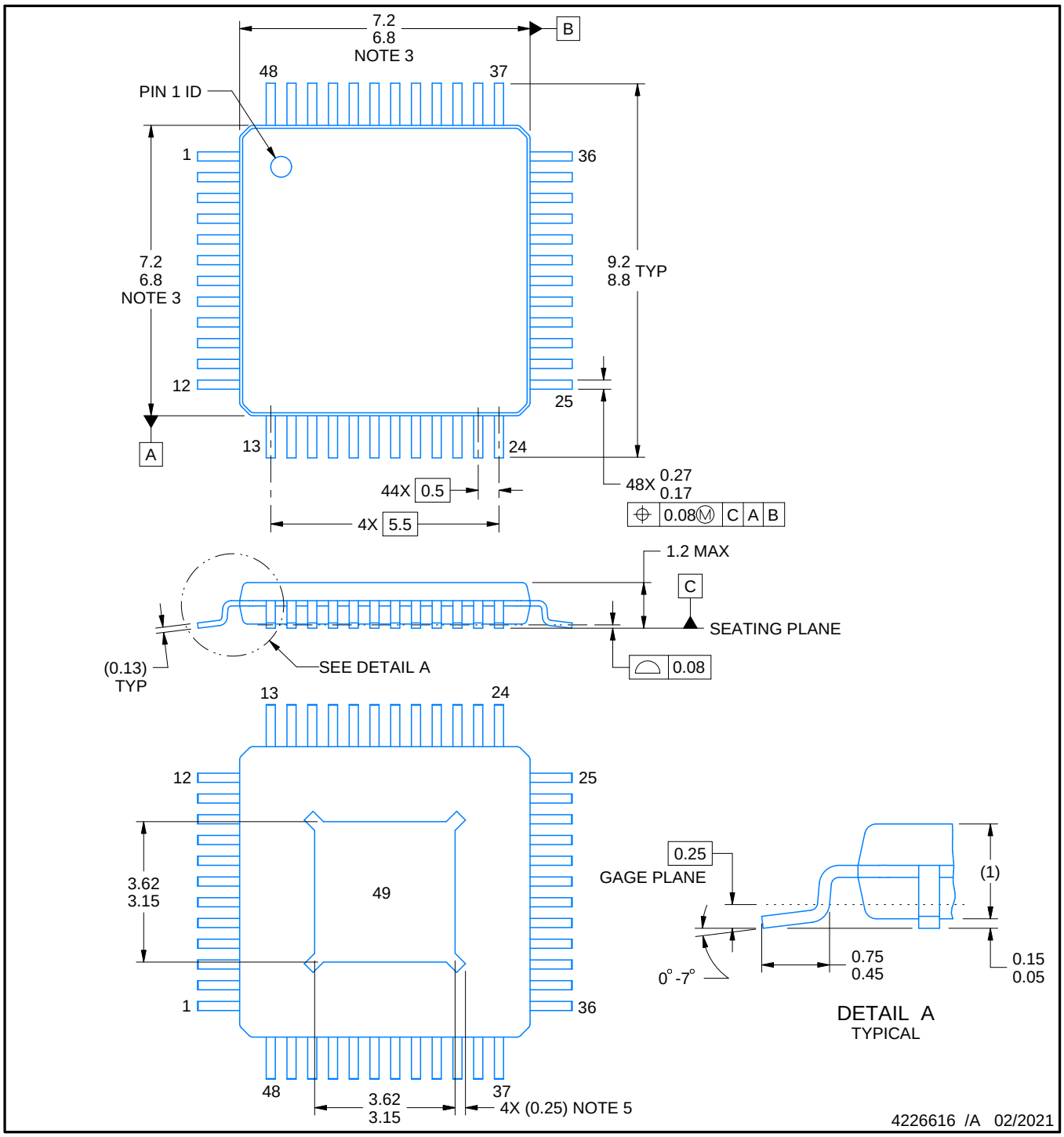


4226443/A

PACKAGE OUTLINE

PHP0048E

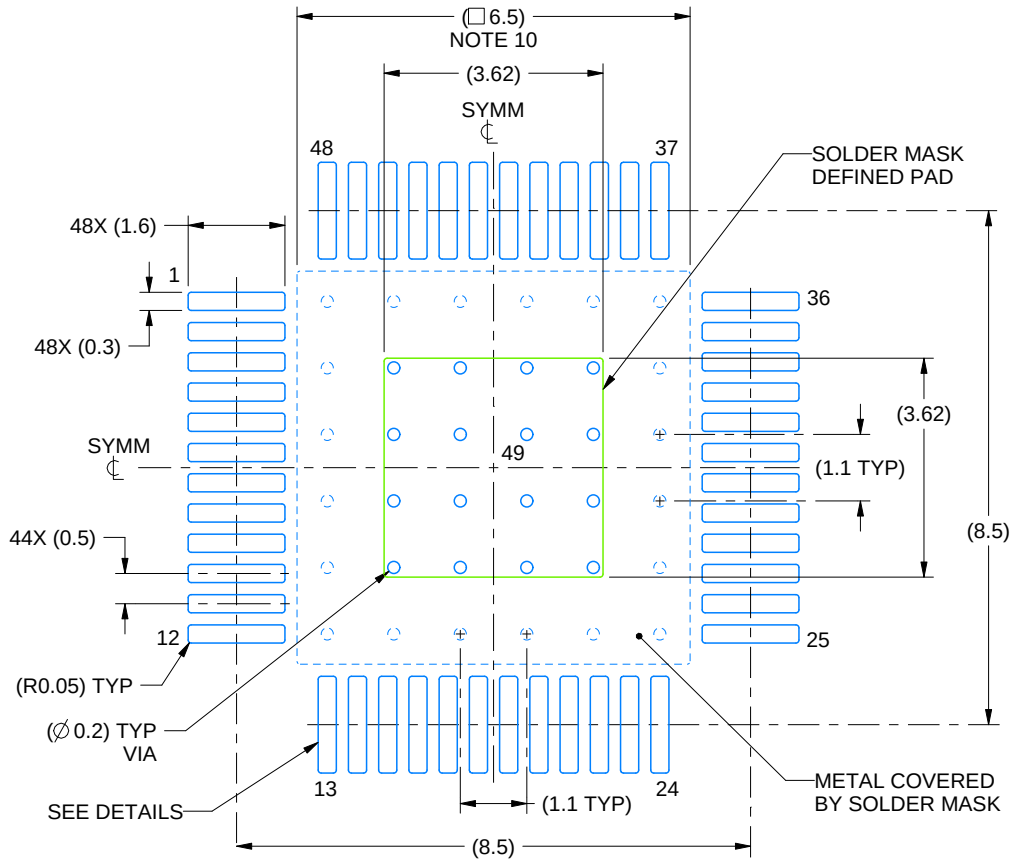
PowerPAD™ HTQFP - 1.2 mm max height



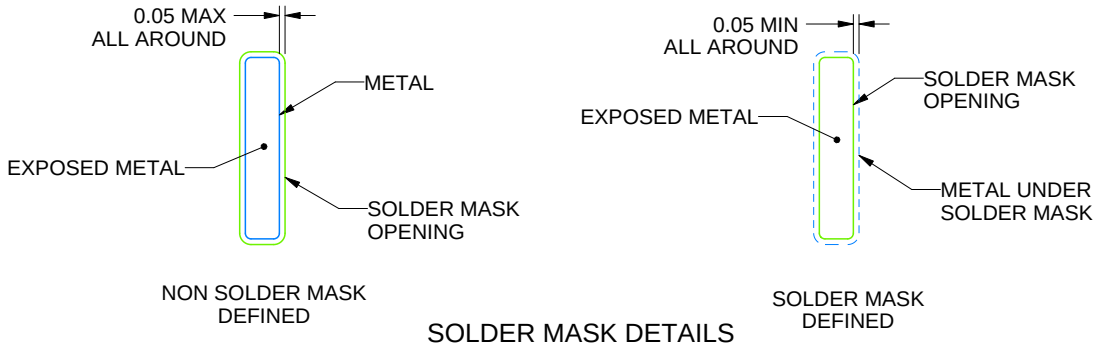
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

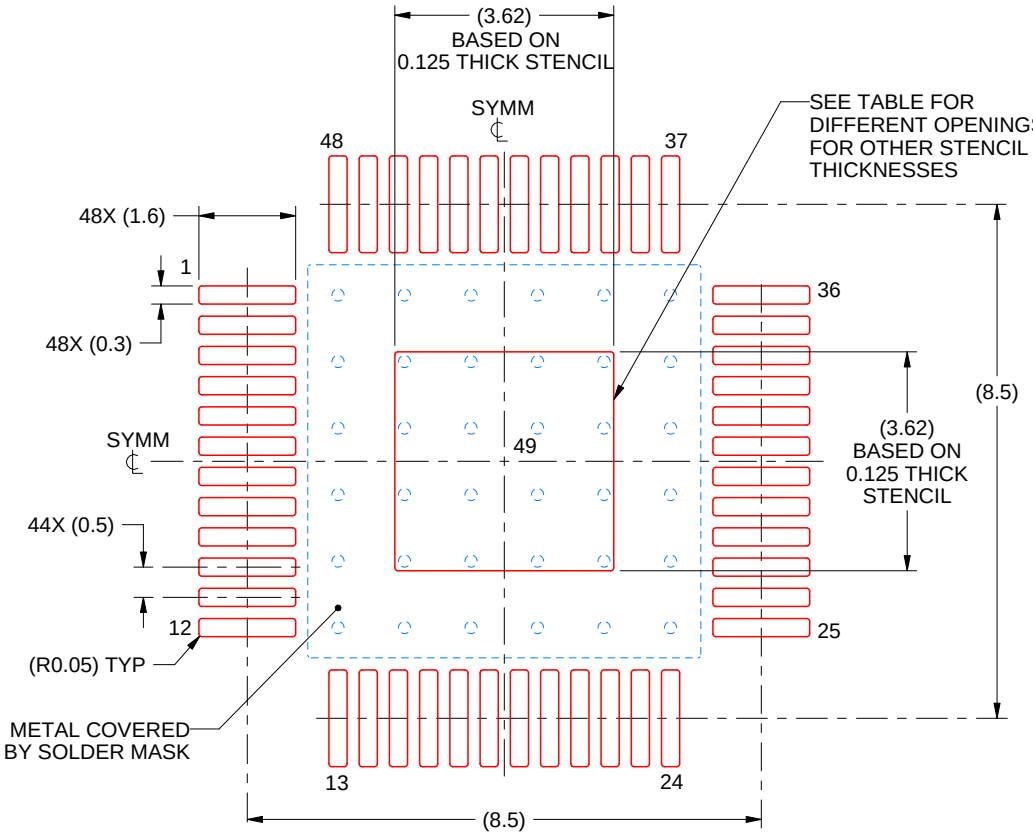


SOLDER MASK DETAILS

4226616 /A 02/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.05 X 4.05
0.125	3.62 x 3.62 (SHOWN)
0.150	3.30 x 3.30
0.175	3.06 x 3.06

4226616 /A 02/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

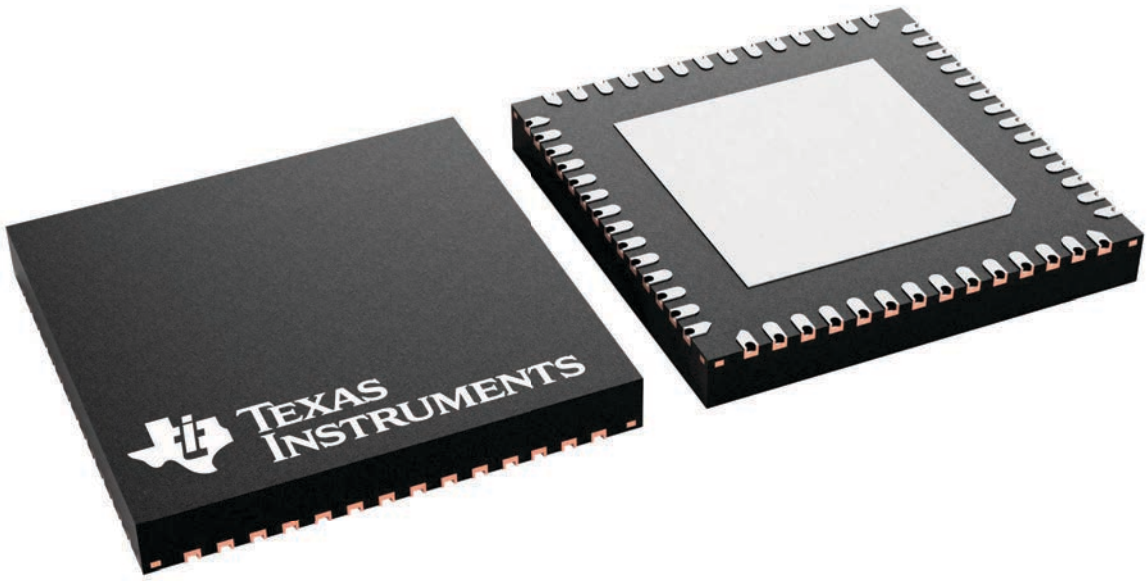
RVJ 56

VQFN - 1 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



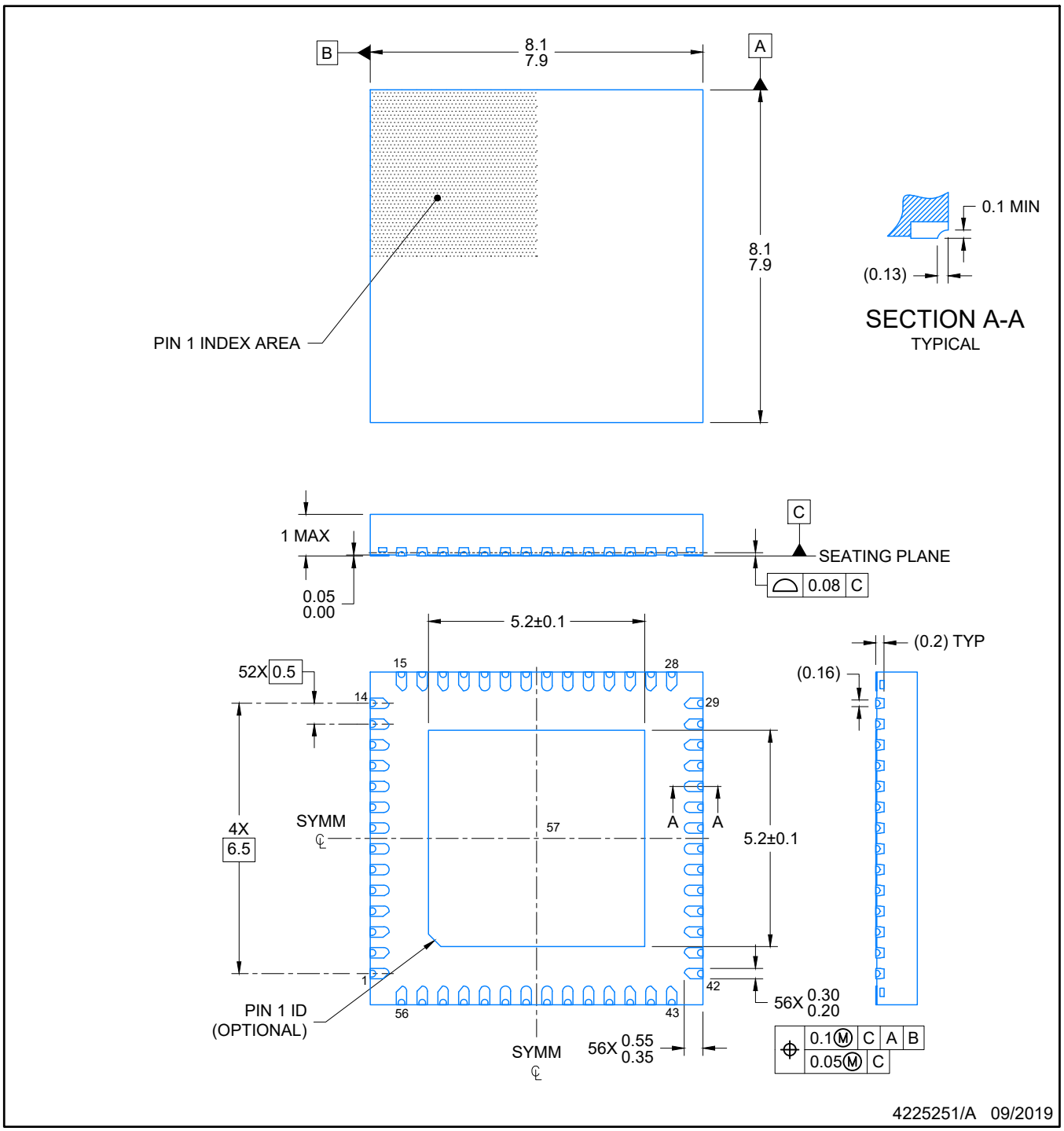
4230924/A

PACKAGE OUTLINE

RVJ0056A

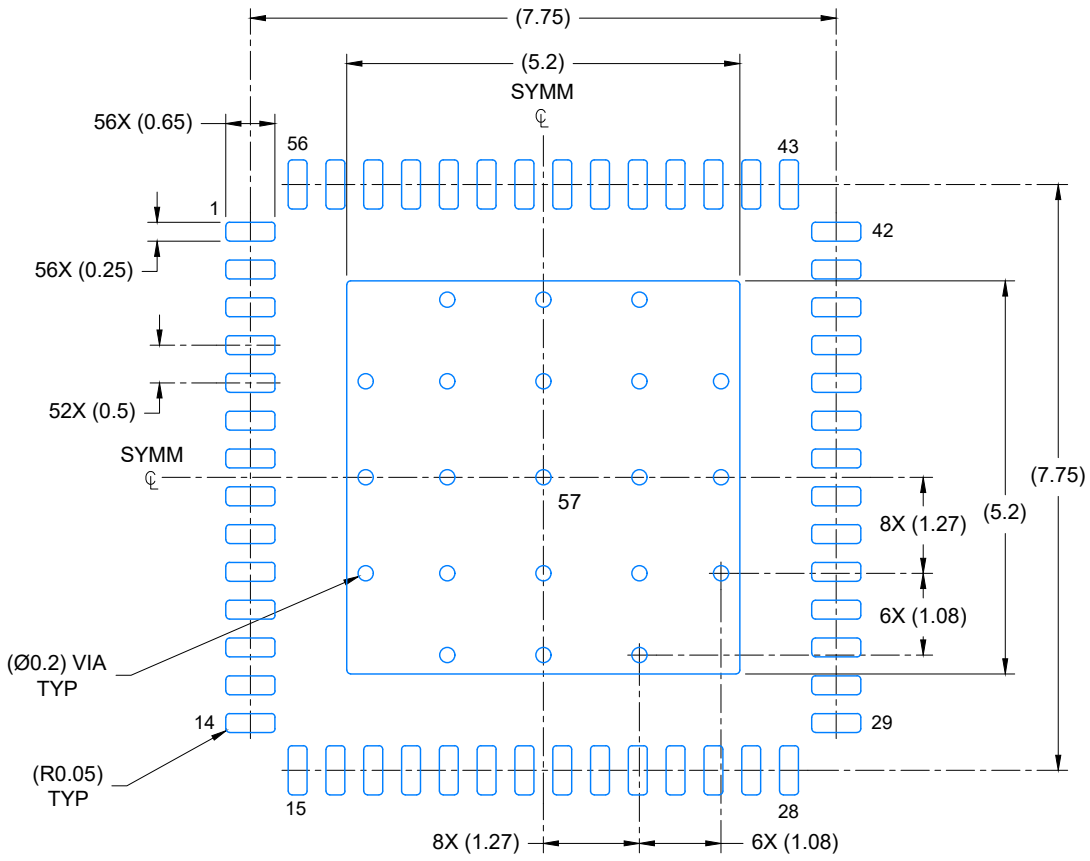
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



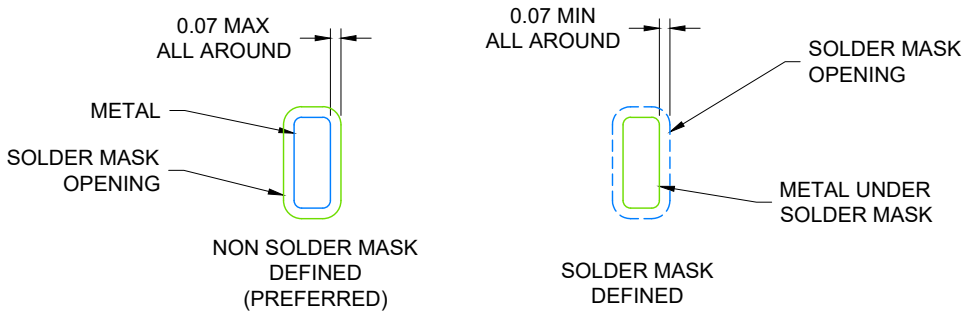
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 10X

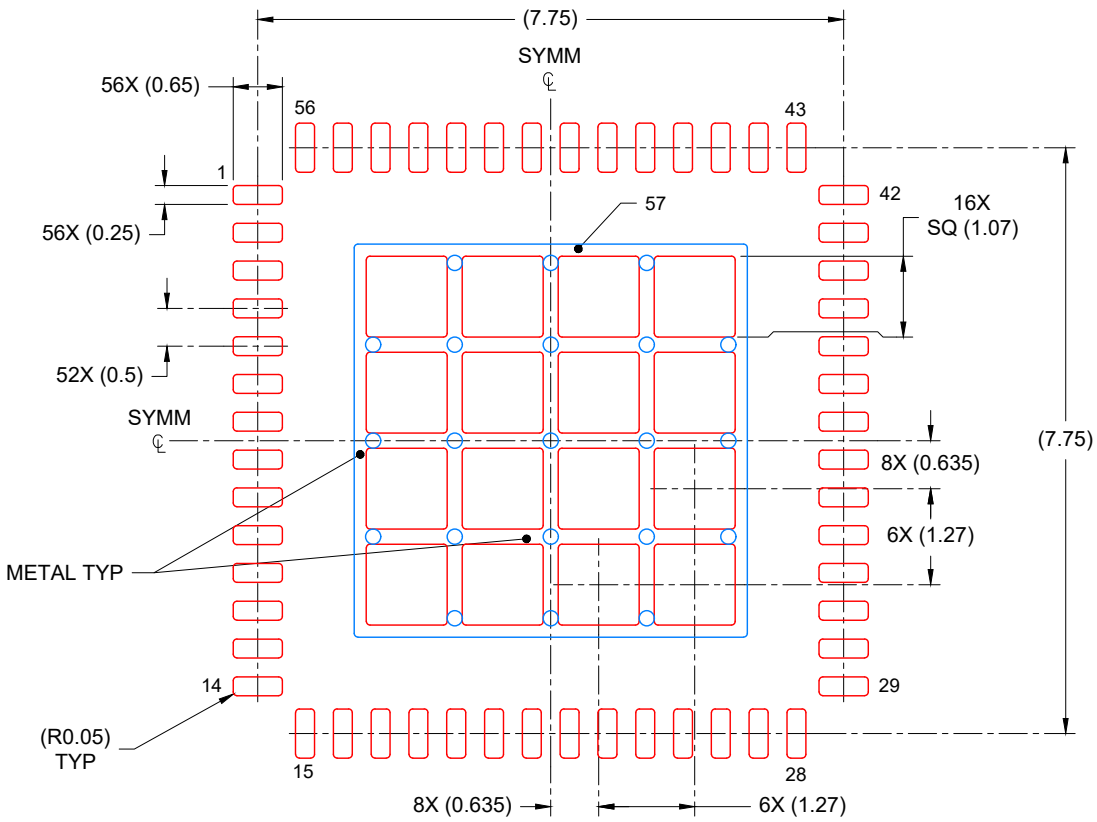


SOLDER MASK DETAILS

4225251/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 10X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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